3.3V Quad Interface, Dual Codec

Advance Information

DS5320 ISSUE 3 June 2002

Features

- Two PCM Codecs (ITU-T G.711/G.712, 8kHz PCM)
- Four Audio TX/RX Interfaces
- Single 3.3V Power Supply
- Flexible Voice Data Port Works in ST-bus, GCI and SSI Modes
- Serial MicroPort Interface Compatible with Motorola and National Semiconductor
- Low External Component Count
- Low Power (43mW typical)
- Power-Down Mode
- Differential Microphone Inputs
- Programmable Bias Voltage Output for Electret Microphones
- Microphone Presence Detection
- Microphone Mute
- Programmable Microphone Gain (0dB to +46.5dB in 1.5dB Steps)
- ITU-T G.712 High-Pass and Low-Pass TX Filtering
- Programmable Sidetone Gain (-39dB to +6dB in 3dB Steps)
- Sidetone Mute
- Differential Earpiece Driver Outputs
- 66mW rms into 32 Ohms

Ordering Information	
MT92303/PR	44 Pin MQFP
-40 to +85° C	

- 150mW rms into 16 Ohms
- Programmable Earpiece Gain (-28dB to +2dB in 2dB Steps)
- Programmable RX Volume Control (-21dB to 0dB in 3dB Steps)
- RX Channel Mute
- ITU-T G.712 Low-Pass RX Filtering
- Programmable/Optional RX Hi-Pass Filter (6 Corner Frequencies in Range 40Hz-400Hz)
- Three PCM Data Formats - 16-bit Linear, companded ITU-T A-law or U-law
- Cross-Point Connects PCM Channels to any of the Four Audio TX/RX Interfaces
- Auxiliary Ringing/Announcement Input (to Loud Speaker Outputs)

Applications

- Digital Telephone Sets
- VoIP Enterprise Telephones

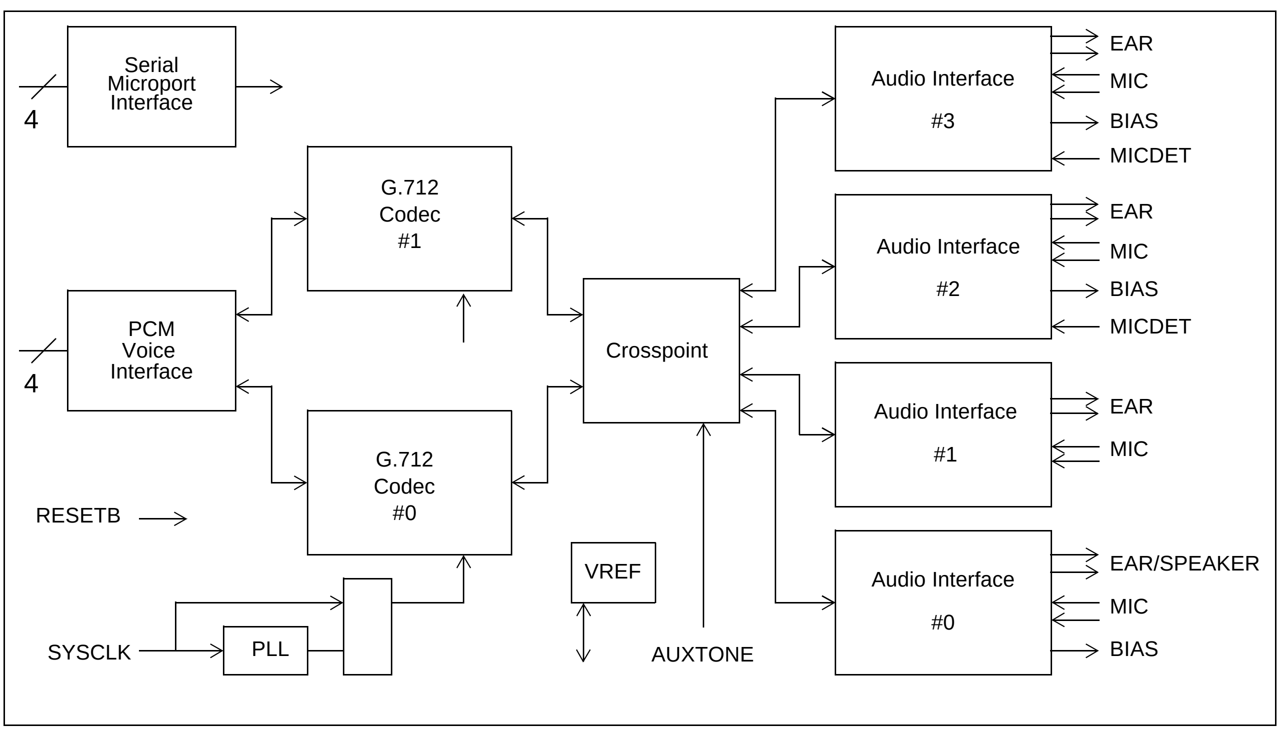


Figure 1 - Block Diagram

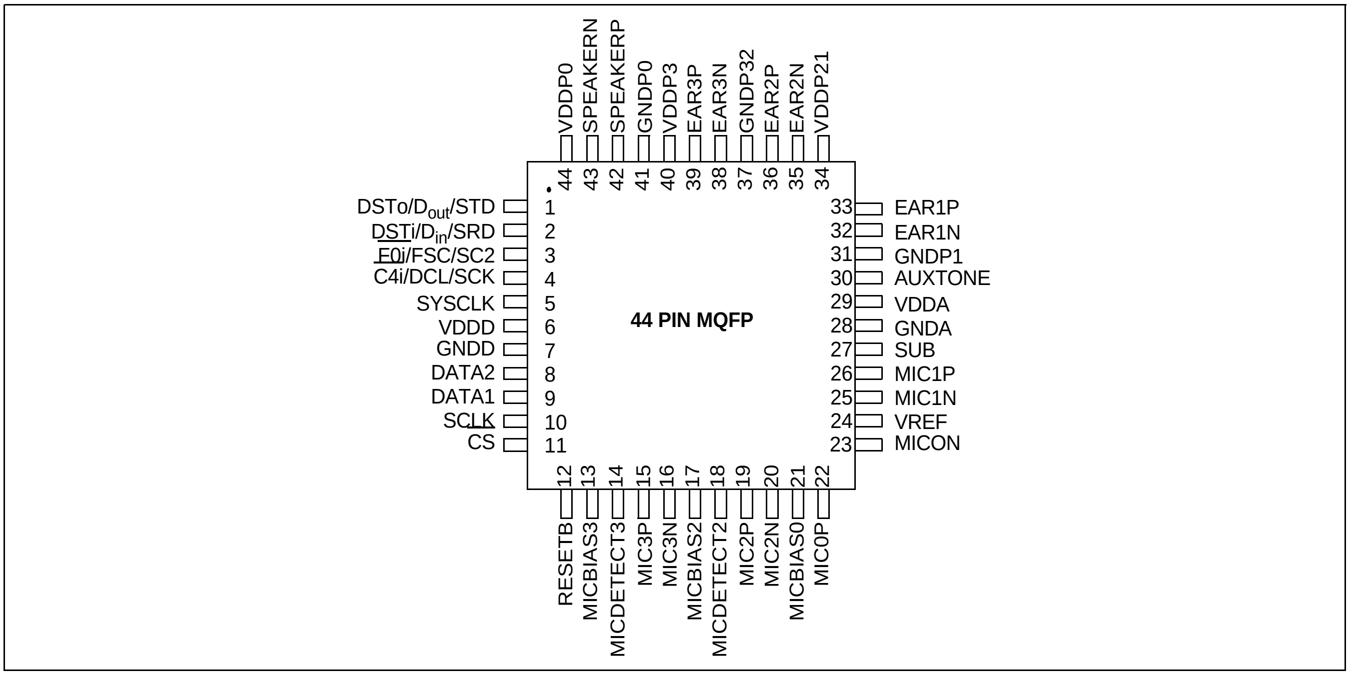


Figure 2 - Pin Diagram

Pin Description

Pin #	Name	Type	Description
			System
5	SYSCLK	Input	Master clock (2.048, 4.096, 10.24, 20.0, 20.48, 25.0 or 50.0MHz)
12	RESETB	Input	Active Low reset signal for digital circuitry
6	VDDD	Power	VDD for Digital circuitry and PLL
7	GNDD	Ground	GND for Digital circuitry and PLL
			PCM Interface
4	C4i/DCL/SCK	Input	Serial clock: ST-Bus = 4.096MHz, GCI = 1.536 - 4.096MHz SSI = 0.512 - 4.096MHz
3	F0i/FSC/SC2	Input	Frame Alignment. ST-Bus active low pulse, GCI active high pulse, SSI active high
2	DSTi/D$_{in}$/SRD	Input	Serial data
1	DSTo/D$_{out}$/STD	Output	Serial data
			Serial Microport
11	CS	Input	Enables serial microport. Active low. Rising edge completes the cycle.
10	SCLK	Input	Data clock for serial microport
9	DATA1	Output	Motorola/National mode: output.
8	DATA2	Input	Motorola/National mode: input.
			Analog
24	VREF	Output	On-chip Voltage-Reference decoupling capacitor, 100nF to GNDA
29	VDDA	Power	VDD for Analog circuitry
28	GNDA	Ground	GND for Analog circuitry
27	SUB	Ground	Chip Substrate (connect to GNDA)

Pin Description (continued)

Audio Interface #3			
13	MICBIAS3	Output	Programmable voltage (0 to 2.5V in 15 steps) for Electret Microphones
14	MICDETECT3	Input	Comparator input to detect Presence & Muting of Microphone
15	MIC3P	Input	Positive Microphone input
16	MIC3N	Input	Negative Microphone input
40	VDDP3	Power	VDD for RX Analog O/P circuitry (Audio Interface #3)
39	EAR3P	Output	Positive Earpiece output
38	EAR3N	Output	Negative Earpiece output
37	GNDP32	Ground	GND for RX Analog O/P circuitry (Audio Interfaces #3 & #2)
Audio Interface #2			
17	MICBIAS2	Output	Programmable voltage (0 to 2.5V in 15 steps) for Electret Microphones
18	MICDETECT2	Input	Comparator input to detect Presence & Muting of Microphone
19	MIC2P	Input	Positive Microphone input
20	MIC2N	Input	Negative Microphone input
36	EAR2P	Output	Positive Earpiece output
35	EAR2N	Output	Negative Earpiece output
34	VDDP21	Power	VDD for RX Analog O/P circuitry (Audio Interfaces #2 & #1)
Audio Interface #1			
26	MIC1P	Input	Positive Microphone input
25	MIC1N	Input	Negative Microphone input
33	EAR1P	Output	Positive Earpiece output
32	EAR1N	Output	Negative Earpiece output
31	GNDP1	Ground	GND for RX Analog O/P circuitry (Audio Interface #1)
Audio Interface #0			
21	MICBIAS0	Output	Programmable voltage (0 to 2.5V in 15 steps) for Electret Microphones
22	MIC0P	Input	Positive Microphone input
23	MIC0N	Input	Negative Microphone input
44	VDDP0	Power	VDD for RX Analog O/P circuitry (Audio Interface #0)
43	EAR0N/SPEAKERN	Output	Negative Earpiece output (high power for Loud Speaker)
42	EAR0P/SPEAKERP	Output	Positive Earpiece output (high power for Loud Speaker)
41	GNDP0	Ground	GND for RX Analog O/P circuitry (Audio Interface #0)
Auxiliary Tone Input			
30	AUXTONE	Input	Auxiliary ringing/announcement input (to Loud Speaker outputs)

Functional Description

The MT92303 Dual Codec provides complete audio to PCM interfaces including filtering and optional data companding as required by the ITU-T G.711 & G.712 recommendations. Programmable gain allows adjustment for a wide range of transducer sensitivities - two microphone amplifiers and four earpiece amplifiers are provided to allow connection to a handset, headset, auxiliary channel and microphone/speaker. A cross-point circuit allows either Codec to be connected to any of the four Audio Interfaces. Programmable voltage sources are available for electret biasing on the Microphone channels.

PCM voice data is passed via a serial interface which operates in ST-bus, GCI or SSI mode. ST-bus mode allows the Codecs to be allocated to any of the 32 available channels. Control and programming of the Codecs is carried out over a flexible, serial, micro-controller interface.

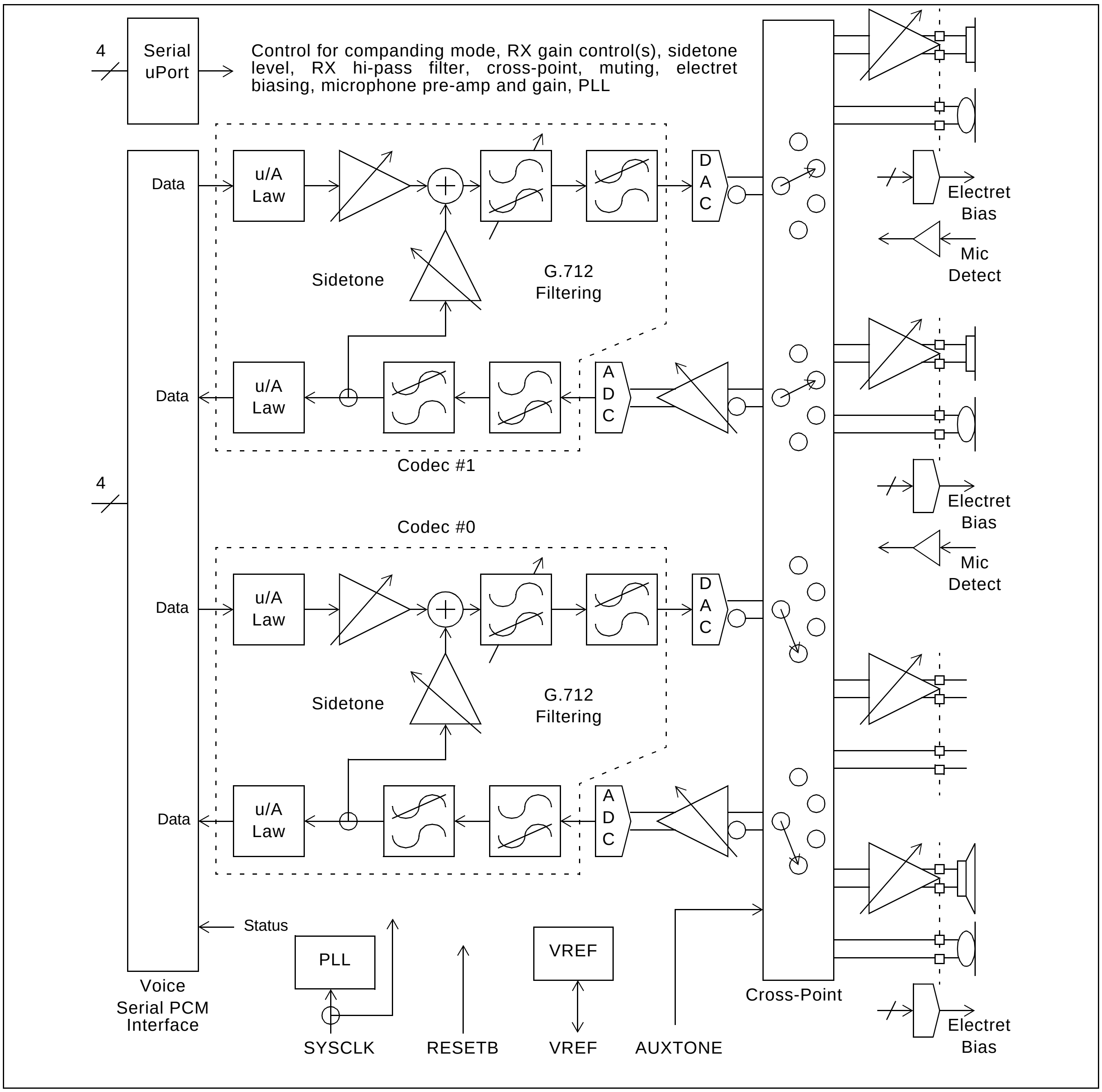


Figure 3 - Block Diagram

Voice Channel

Figure 4 shows the companding, filtering and gain stages in a single voice channel as set up by the Cross-Point. The RX channel (top) and TX channel (bottom) both use a mixture of digital-DSP and analog techniques. The DSP domain is towards the left of the diagram and extends from the PCM interface to the DAC and ADC blocks.

RX Channel

PCM data is taken in either linear or companded form and is processed by the DSP circuitry. This provides a digital volume control, an access point for sidetone, and the multi-order low-pass filtering required to remove the sampling aliases in the digitized data. The 6^{th} order low-pass filter response is shown in Figure 5. An optional 1^{st} order high-pass filter is also provided. In addition to the gain adjustment, the RX DSP channel may also be turned-off (‘muted’). The filtered version of the data is converted to an analog signal by the DAC and continuous-time low-pass filter before passing through the Cross-Point circuitry to the variable-gain output buffer. The buffer provides a differential output signal which allows near rail-to-rail operation and can deliver 66mW into a 32 Ohm load.

As shown in Figure 4, the RX gain may be adjusted in two places. The ‘DSP’ provides adjustment from -21dB to +0dB in 3dB steps, and the ‘analog’ from -28dB to +2dB in 2dB steps.

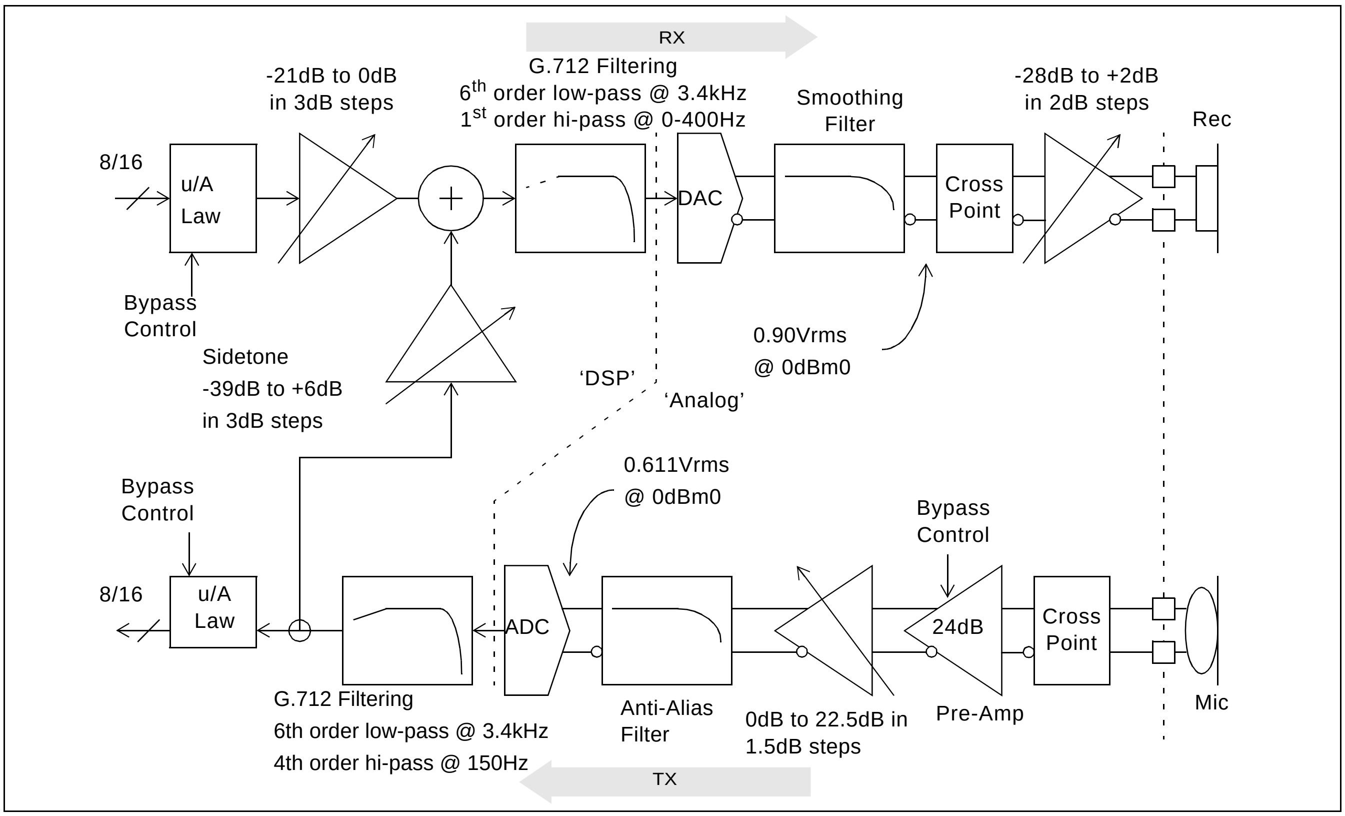


Figure 4 - Single Voice-Channel DSP and Analog Circuitry

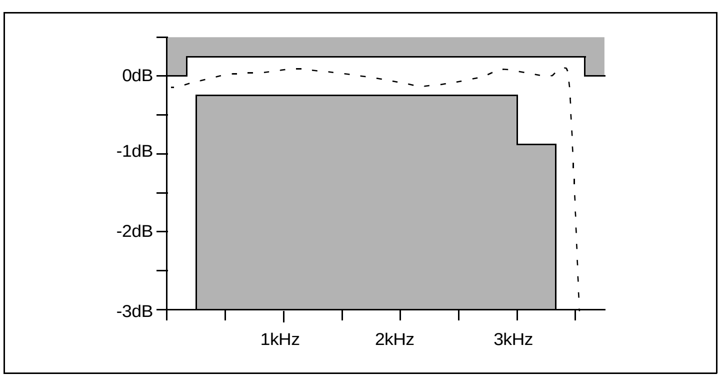


Figure 5 - RX Low-Pass Filter Response

Loud Speaker Drive

The MT92303 provides four Audio Interfaces, all of which provide the same gain adjustments and output drive voltage levels. However, Audio Interface #0 has an output buffer which is capable of delivering more current than the others, and is intended for use with a loud speaker. This output can drive 150mW r.m.s. into a 16 Ohm load - this represents almost rail-to-rail operation from the 'bridge' configured outputs. The four buffers each have the same output resistance - typically 1 Ohm.

Other loud speaker impedances may be used (as long as they are greater than or equal to 16 Ohms) and will allow a power output (t.h.d. < 1%) of:

- Power = 150mW x 16 / Rload

The MT92303 can be used with loud speaker impedances below 16 Ohms, but should not be allowed to provide extra drive current by doing this. The Loud Speaker Driver is designed to deliver sufficient current to maintain a maximum amplitude signal across a 16 Ohm load - exceeding this current may cause long-term damage to the device. If impedances below 16 Ohms are used, then the 'RX Analog Gain' should not be set to maximum. For example, an 8 Ohm loud speaker should be used with gains which are at least 6dB below the maximum. It should be noted that in this example, the electrical power delivered to the 8 Ohm load is less than that delivered to a 16 Ohm load at maximum gain.

TX Channel

An optional pre-amp and a variable gain stage provide a very large range of gain adjustment for the microphone signal. The boosted signal is passed through an anti-alias filter before it is digitized by the ADC and routed to the DSP circuitry. The DSP band-pass filtering provides a sharp cut-off above 3.4kHz to prevent aliasing by the 8kHz sampling, and also provides a high-pass function at 150Hz to remove low-frequency voice energy.

As shown in Figure 4, the pre-amp and variable gain block combine to allow the TX gain to be adjusted from 0dB to +46.5dB in 1.5dB steps.

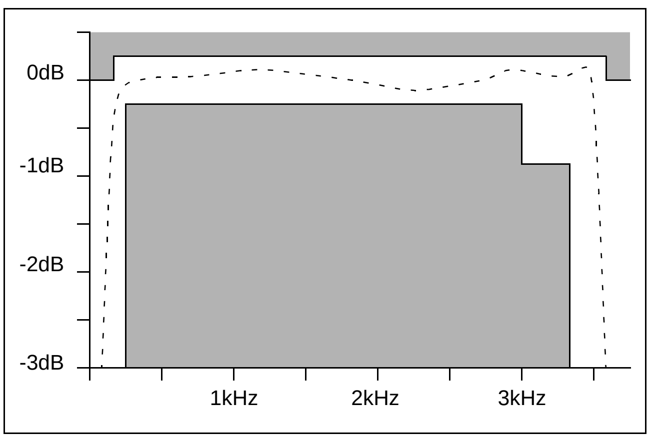


Figure 6 - TX Band-Pass Filter Response

The 8kHz samples are available in either 16-bit linear form, or 8-bit u-Law or A-Law companded form.

The differential amplifiers may be used with electret microphones as shown in Figure 8, or with dynamic microphones which have no bias requirements. Even though they require no d.c. biasing, dynamic microphones must still be connected to the chip inputs with a coupling capacitor.

DC offset voltages which potentially exist on the amplifier inputs are automatically cancelled by a sequence which runs each time the circuit is powered-up (see section 'Automatic DC Offset Cancellation').

The ‘Mic’ inputs of the TX channel have a differential input impedance which is sufficiently high to allow the use of small value coupling capacitors. The input impedance is formed by the internal gain-setting resistors which are used around the op-amps, and consequently the value of the input impedance is dependent on the selected gain as shown in Table 1.

Input Impedance‡ (kOhms)			
Gain	**Min**	**Typ**	**Max**
0dB to 10.5dB	49	107	213
12dB to 22.5dB	29	54	89
24dB to 46.5dB	52	80	113

‡ These figures are for design aid only: not guaranteed and not subject to production testing.

Table 1 - Microphone Input Impedance

Automatic DC Offset Cancellation (TX)

The amplifiers in the TX channel can provide gains as high as 46.5dB (linear gain of x211). Potential DC input offset voltages on the amplifier inputs need to be controlled so that they do not affect the dynamic range of the channel. These DC offset voltages are removed by a sequence which automatically runs each time the TX ‘analog’ circuitry is enabled/powered-up (see control register ‘Audio Interface: Enable’).

The ‘offset cancellation’ routine works by using internal DACs to introduce small correction voltages into the amplifiers so that their outputs have a nominal DC level of 0V (measured differentially). The digital portion of this auto calibration circuitry is clocked by the ‘Frame Alignment’ input and requires up to 128 clock pulses. It is important that the on-chip voltage reference is powered-up and allowed to settle before the ‘offset cancellation’ is initiated (by enabling the TX ‘analog’ circuitry).

There are two TX ‘analog’ channels, each of which has its own ‘offset cancellation’ circuitry. These can operate completely independently of each other if required.

It is recommended that the programming sequence used for the MT92303 is arranged such that the ‘offset cancellation’ routine is run each time a new ‘call’ is setup. In this way, the offset correction will be able to track any ‘drift’ in operation of the MT92303 over its lifetime.

Sidetone Path

The DSP circuitry provides a path between the TX and RX channels for the adjustment of sidetone level. In addition to the large range of adjustment, the sidetone may also be turned-off (‘muted’).

As shown in Figure 4, the sidetone gain may be adjusted from -39dB to +6dB in 3dB steps.

Auxiliary Tone Input

A separate analog input to the Loud Speaker Driver (Audio Interface #0) is provided for the purpose of sending auxiliary ringing/announcement tones to the loud speaker. This input (‘AUXTONE’) allows analog signals to be buffered by the programmable-gain driver circuit. The AUXTONE path is not normally connected, and needs to be selected by the appropriate bits in the Cross-Point control register. The analog gain from AUXTONE to the SPEAKERP/N pins is defined by the same register as for ‘RX Analog Gain’ in Audio Interface #0, and is adjustable between -26.5dB and +5.9dB in approximate steps of 2dB.

The maximum undistorted signal which can be generated by the SPEAKERP/N pins has a ‘peak’ amplitude of approximately VDD-1 e.g. 2.3V peak, or 4.6V peak-peak, for a 3.3V supply. It should be noted that a combination of large input signal and maximum AUXTONE gain can cause the output signal to ‘clip’.

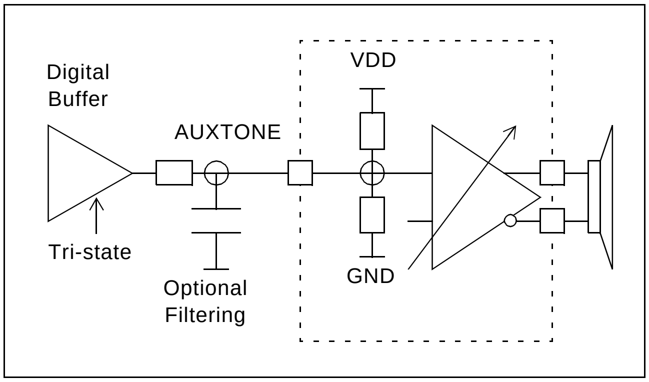


Figure 7 - AUXTONE Circuitry

The AUXTONE input may be driven by a true analog source (e.g. op-amp) or a pseudo-analog signal provided by a ‘digital’ driver as shown in Figure 7. For minimum external component count, the digital driver should go high-impedance when not in use (to minimize ‘clicks’ and ‘pops’).

The AUXTONE input is DC biased at VDD/2 and should be capacitively coupled to sources with a different DC level.

Cross-Point

Any 2 of the 4 RX Earpiece drivers may be selected for connection to the 2 Codecs. Similarly, any 2 of the 4 Microphones may be selected for connection to the 2 Codecs. This is done via the ‘cross-point’ and is controlled by the appropriate register. The same register contains two ‘CON_CODEC’ bits which must be ‘set’ in order to establish any connection to the Codecs. These bits allow the Codecs to be completely disconnected from the Audio Interfaces (the default state after System reset).

In the event of both Codecs being erroneously selected for connection to one of the Earpiece/Microphone circuits, then Codec #0 will take priority.

In the event of one of the Codecs being selected for connection to Earpiece #0 (the driver designated for the Loud Speaker), and the simultaneous selection of the AUXTONE input, then the AUXTONE path will take priority.

Special Cross-Point Modes

The cross-point is normally used to setup one or two channels, each of which consists of a Microphone circuit, a Codec, and an RX Earpiece driver. However, there are two special modes in which **two** Earpiece drivers may be connected to the same Codec (only Codec #0).

These special ‘Dual Output’ modes are controlled by the ‘OVERRIDE’ bits in the ‘Cross-Point: Selection’ register as shown in the following table.

OVER RIDE	Cross-Point Operation
00	Normal Mode
01	AUXTONE to Loud Speaker Output (EAR #0). Overrides XP0/1
10	Dual Output Mode 1: EAR#3 (master) and EAR #0 connected to Codec #0
11	Dual Output Mode 2: EAR#2 (master) and EAR #3 connected to Codec #0

Table 2 - Special Cross-Point Modes

Notice that one of the Earpiece drivers is designated as ‘master’ when in ‘Dual Output’ mode. This means that the ‘master’ must also be selected for connection to Codec #0 (by the other control bits in the ‘Cross-Point: Selection’ register).

Electret Bias

Programmable output voltages are available on three of the Audio Interfaces - these are provided for the biasing of electret microphones as shown in Figure 8.

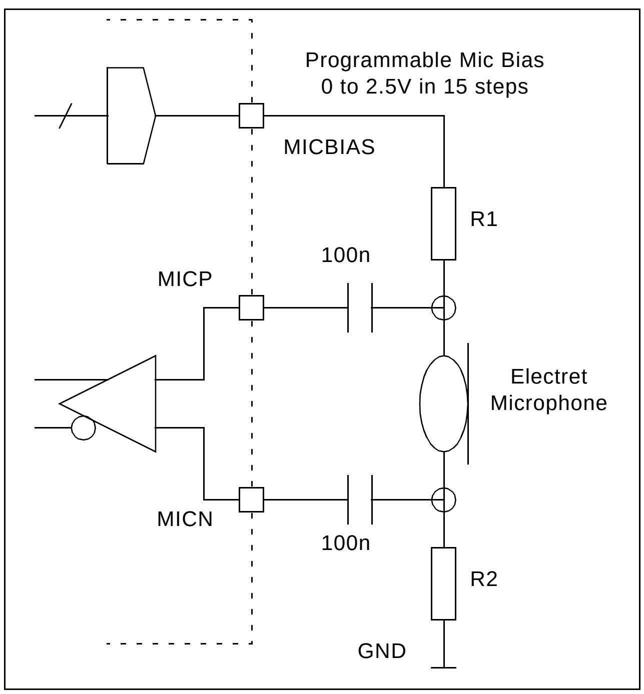


Figure 8 - Programmable Electret Bias

The electret bias is programmed via one of the control registers, and provides a stable, low noise voltage which is derived from the on-chip voltage-reference. The bias voltage is programmable from 0 to 2.5V (nominal) in 15 steps, and has a nominal output noise level of 25uV (rms, 300-3400Hz).

Notice that almost all of the noise from the electret bias generator appears across the microphone. When the TX/Mic gain is set towards its maximum value, the signal-to-noise performance will be affected by the noise from the bias generator.

Microphone Presence Detect

When an electret microphone is connected as shown in Figure 8 and Figure 9, it draws a bias current from the MICBIAS pin. The voltage across the 'bottom' bias resistor is monitored by the MICDETECT input and is used to set a 'presence' flag in the MT92303's Status Register. This allows the external controller to determine whether or not the handset and headset are plugged-in. The internal workings of the MT92303 are not affected by the state of the 'presence' flag.

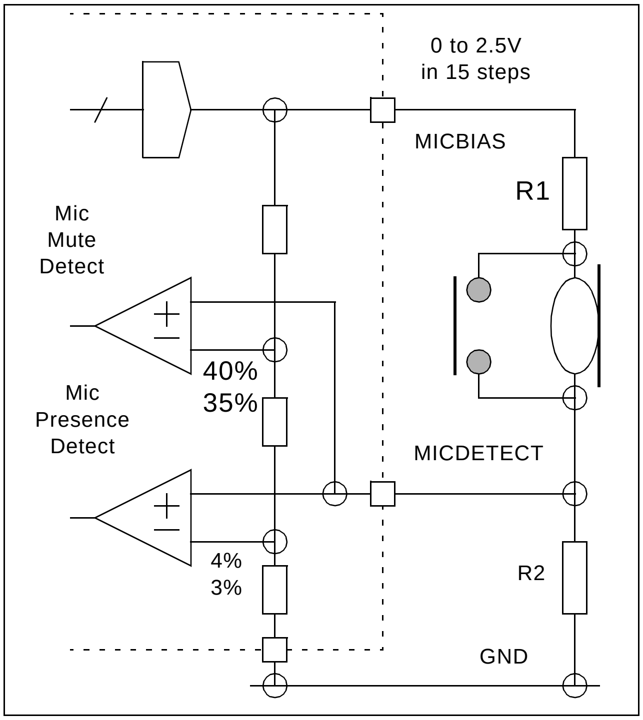


Figure 9 - Mic Presence and Mute Detect

Microphone Mute Detect

Any of the 4 Microphone inputs can be 'muted' under direct software control via the 'Mode Control' register.

In addition, the MICDETECT inputs may also be used to mute the microphone paths of the 2 associated Audio Interfaces. This allows instantaneous blanking of the microphone path, and consequently the sidetone path, and allows the 'pop' associated with electret muting to be avoided.

As shown in Figure 9, the internal 'Mic Mute Detect' signal is activated whenever the voltage across the 'bottom' bias resistor (R2) exceeds 40% of the MICBIAS voltage. A small amount of hysteresis is implemented such that the voltage needs to fall below 35% of the MICBIAS voltage before the internal 'Mic Mute Detect' signal is deactivated.

In addition to internally muting the microphone channel, the 'Mic Mute Detect' signal is passed to the MT92303's Status Register.

The behavior of the mute function can be programmed to operate in four different ways.

MUTE MODE	Mute Operation (see Figure 9)
00	Microphone path enabled (normal operation). ‘Mic Mute Detect’ signal ignored.
01	Microphone path disabled (muted) while ‘Mic Mute Detect’ signal is high, and enabled while low.
10	Microphone path disabled (muted) while ‘Mic Mute Detect’ signal is high, **but must be re-enabled by the external controller**.
11	Microphone path disabled (muted). ‘Mic Mute Detect’ signal ignored.

Table 3 - Microphone Mute Detection

It is important to note that in the third mode (MUTEMODE=10) described in Table 3, it is the designer’s responsibility to re-enable the microphone path after it has been muted by the MICDETECT pin. This allows the designer to re-establish the signal path after a time sufficient for the settling of any microphone bias circuitry.

The on-chip ‘Status’ register provides access to the internal ‘Mic Mute Detect’ signal, and also the acknowledged version ‘Mute’ which denotes whether or not the microphone channel is actually muted. These two bits of information are expected to be used by the external controller to determine when the channel needs to be re-enabled. This will be when ‘Mute’ is high, and ‘Mic Mute Detect’ has fallen low, but the external controller may introduce a delay before re-establishing the microphone path. The path should be re-enabled by momentarily switching to MUTEMODE=00.

Designation of Audio Interfaces

As already described, the MT92303 has four Audio Interfaces which are very similar to each other. The following summary of the **differences** should be useful in the early stages of design, when the Interfaces are being designated their specific tasks.

- MIC #1 is the simplest interface, and has no electret bias facility, or microphone ‘detect’ circuitry.
- MIC #0 has no microphone ‘detect’ circuitry.
- EAR #0 has a higher drive capability, and may be used for a loud speaker.
- EAR #0 may be connected to an ‘external’ signal via the AUXTONE pin.
- Codec #0 may be used in special ‘Dual Output’ modes, but #1 may not.
- EAR #3 and #0 may be driven simultaneously by the same signal (Codec #0) in a special ‘Dual Output’ mode.
- EAR #2 and #3 may be driven simultaneously by the same signal (Codec #0) in a special ‘Dual Output’ mode.

Bandgap Voltage Reference

The MT92303 has its own internal bandgap voltage reference which determines the absolute gains of the TX & RX paths. The bandgap voltage is brought out to the VREF pin for external decoupling with a capacitor (100nF to GNDA) that should be located as close to the package as possible. The bandgap voltage has a nominal value of 1.26V and may be used by other external circuitry as long as this is not allowed to interfere with the reference voltage. The reference voltage is not designed to deliver current so it should not be connected to a resistive load, or an AC noise source which cannot be decoupled by the external capacitor alone.

The reference voltage circuit may be powered up and down under the control of one of the internal registers. When it is powered up, the reference voltage will take <1ms to settle.

PCM Interface (Voice & Status)

The TX and RX digitized voice data is accessed via the PCM interface which can be programmed to work in one of three modes. These are ST-bus, GCI and SSI mode as described below. The contents of an on-chip ‘Status’ register may also be read via this interface.The DSTo/Dout/SDT pin is high impedance when inactive - this allows multiple codecs to share the PCM bus.

Pin Name	Type	Description
$\overline{\text{C4i}}$/DCL/SCK	Input	Serial clock. ST-Bus = 4.096MHz GCI = 1.536 - 4.096MHz SSI = 0.512 - 4.096MHz
$\overline{\text{F0i}}$/FSC/SC2	Input	Frame Alignment. ST-Bus active low pulse GCI active high pulse SSI active high
DSTi/D_{in}/SRD	Input	Serial data
DSTo/D_{out}/STD	Output	Serial data

Table 4 - PCM Interface Pin Description

PCM codes which are equivalent to a ‘digital mW’ (0dBm0) for a 1kHz sinewave are shown in Table 5. ITU-T G.711 defines the peak coding level for A-law as 3.14dBm0 and for u-Law as 3.17dBm0.

Phase	A-Law	u-Law	Linear
-7/8	00110100	00011110	1101110110000100
-5/8	00100001	00001011	1010111010000100
-3/8	00100001	00001011	1010111010000100
-1/8	00110100	00011110	1101110110000100
1/8	10110100	10011110	0010001001111100
3/8	10100001	10001011	0101000101111100
5/8	10100001	10001011	0101000101111100
7/8	10110100	10011110	0010001001111100
-Full	00101010	00000000	1000000000000000
Zero	11010101	11111111	0000000000000000
+Full	10101010	10000000	0111111111111111

Table 5 - PCM Coding

The A-law and u-Law schemes use sign-magnitude data, and the Linear system uses 2’s compliment. The data words are shown as MSB first.

Table 5 also shows the coding for full-scale and ‘zero’ (‘quiet code’).

PCM ST-Bus Interface

The ST-BUS consists of output (DSTo) and input (DSTi) serial data streams, a synchronous clock input signal (C4i), and a framing pulse input (F0i). These are shown in Figure 10. The data streams operate at 2048 kb/s and are Time Division Multiplexed into 32 identical channels of 64 kb/s bandwidth. A frame pulse (a 244 nSec low going pulse) is used to parse the continuous serial data streams into the 32 channel TDM frames. Each frame has a 125 uSecond period translating into an 8 kHz frame rate. Data is arranged MSB first. A valid frame begins when F0i is logic low coincident with a falling edge of C4i. Refer to Mitel applications note MSAN-126 for detailed ST-BUS timing. C4i has a frequency (4096 kHz) which is twice the data rate. This clock samples the incoming data on DSTi at the 3/4 bit-cell position (the second rising clock edge) and makes data available on DSTo at the start of the bit-cell. A bit cell is the 2 clock cycles used to transfer 1 data bit. See Figure 17 in the electrical characteristics section for detailed timing information.

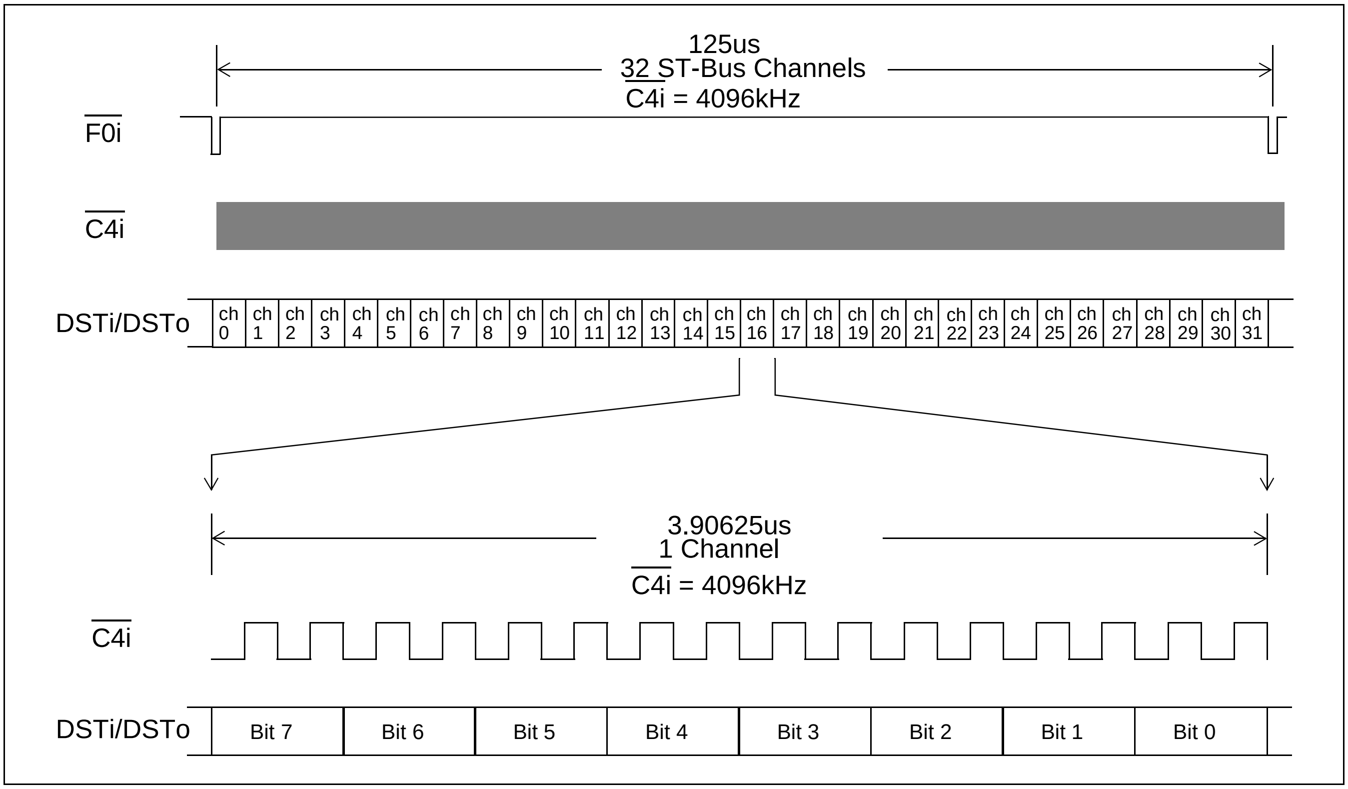


Figure 10 - PCM ST-Bus Channel Allocation in a Frame Pulse

Channel Definition (ST)

Each Codec requires 1 (companded PCM) or 2 (linear PCM) channels. In addition to these 2 or 4 channels there is a ‘status’ channel. The allocation of these channels is fully programmable, subject to the following:

- Data-in and data-out are in the same channel slot for the DSTi and DSTo streams.
- In 16bit linear mode the 2 bytes are in adjacent channels.

This will allow multiple MT92303s to share the ST-Bus (10 in companded and 6 in linear mode).

In the event of the codecs or the status register erroneously having the same channel allocation, the prioritisation is (highest first): codec0, codec1, status. Only the highest priority has access to the PCM channel.

PCM General Circuit Interface (GCI)

In GCI mode the number of channels available in a 125us frame pulse period depends on the DCL clock frequency, a DCL clock frequency of 1536kHz allows 3 channels, 2048kHz allows 4 channels and 4096kHz allows 8 channels.

Each channel is allocated 4 consecutive bytes which are defined as:

- PCM data bytes B1 and B2.
- Monitor byte (M).
- Control/Indication byte (C/I).

For the MT92303 only the B1 and B2 bytes are used, during the M and C/I bytes, Dout is tristate. The serial data streams are Din and Dout, the clock is DCL and the frame pulse is FSC, as shown in Figure 11. Data is arranged MSB first.

The channels selected must be compatible with the DCL clock frequency being used. The ‘status’ register information is also output on one other channel, in the B1 slot. GCI mode is enabled by setting the appropriate bits in the control register.

The clock rate for GCI is double the bit rate. See Figure 18 in the electrical characteristics section for detailed timing information.

Channel Definition (GCI)

The PCM data will be output on the channels defined by the Channel Allocation Registers. The Status register is also output on one other channel on B1 as defined by the Status Channel Allocation Register. No error checking is done so the channels defined must be compatible with the DCL clock frequency.

In the event of codecs or status reg. erroneously having the same channel allocation, the prioritisation is (highest first): codec0, codec1, status. Only the highest priority has access to the PCM channel.

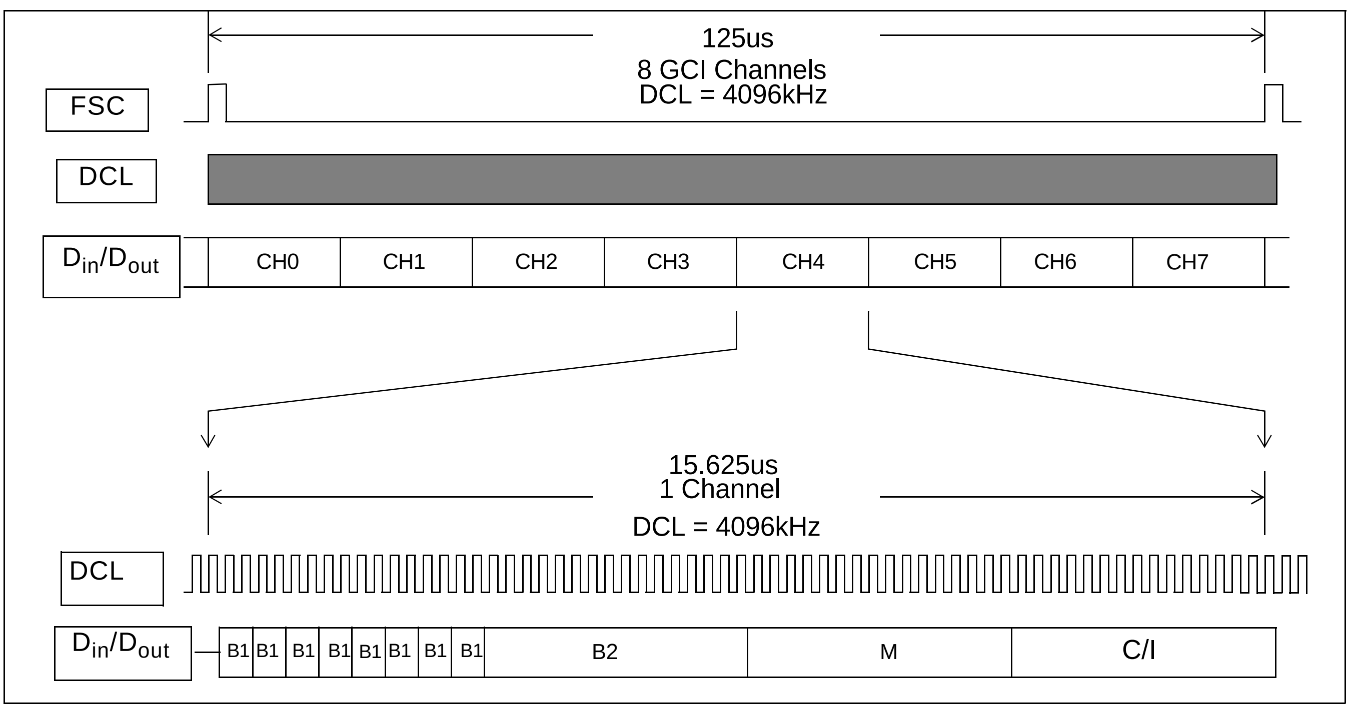


Figure 11 - PCM GCI Channel Allocation in a Frame Pulse

PCM Synchronous Serial Interface (SSI)

This is a commonly used standard in North America. There is no predefined number of bits in a 125us period, instead data is transmitted while the serial chip select pin SC2 is high. Data is input on SDR, being sampled on the falling edge of SCK, data is output on SDT on the rising edge of SCK. Data is arranged MSB first. The clock rate for SSI is the same as the bit rate. See Figure 19 in the electrical characteristics section for detailed timing information.

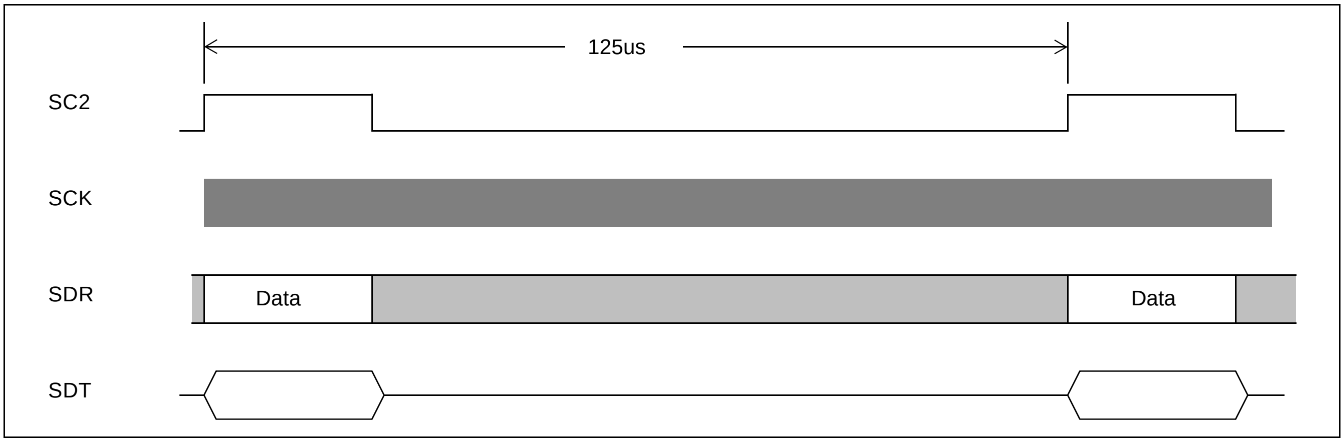


Figure 12 - PCM Synchronous Serial Interface (SSI)

Channel Definition (SSI)

In dual codec mode, codec0 data is transmitted first, either as 8-bit companded or 16-bit linear, then codec1 data and finally the status register. In single codec mode, the codec data is transmitted first and then the status register.

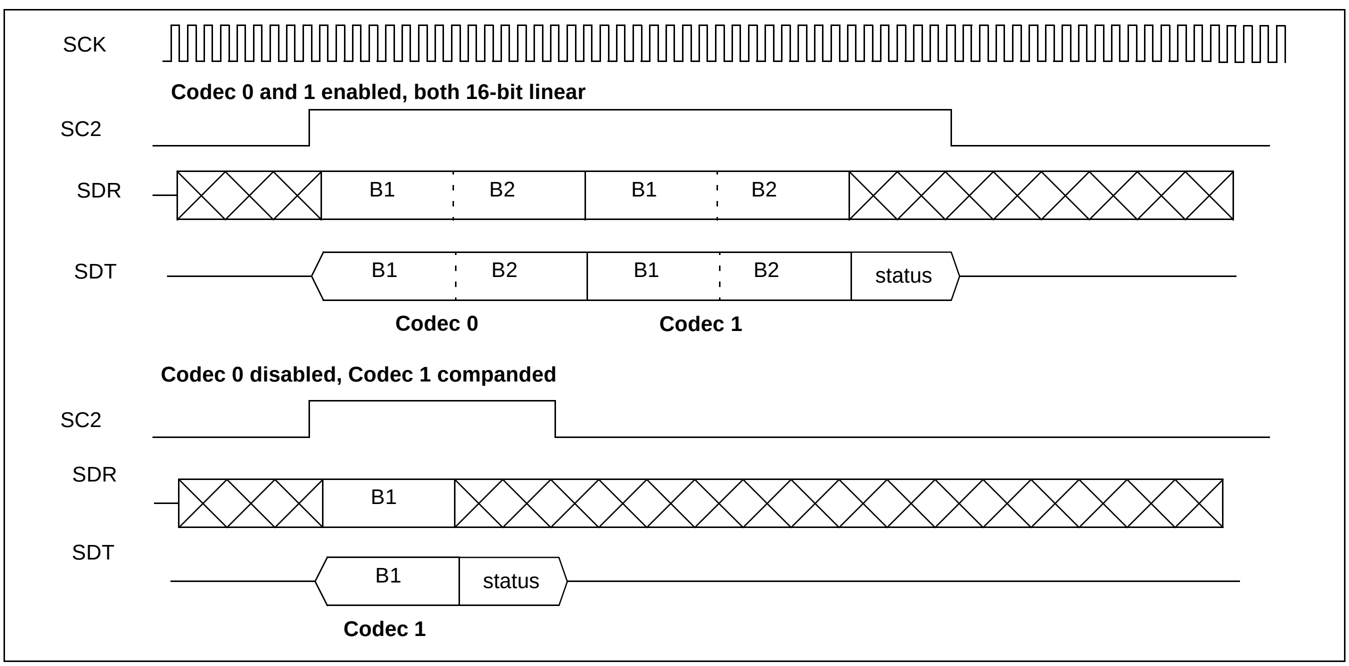


Figure 13 - PCM SSI Bit Allocation

Serial Microport

All MT92303 internal registers are accessed for write via the serial microport to allow programming of the device. In addition some registers may be read via this interface as defined in the ‘Programming and Registers’ section.

Pin Name	Type	Description
$\overline{CS}$	Input	Enables serial microport. Active Low. Rising edge completes the cycle.
SCLK	Input	Data clock for serial microport
DATA1	Output	Motorola/National mode: DATA1 is output.
DATA2	Input	Motorola/National mode: DATA2 is input.

Table 6 - Microport Pin Description

The serial microport is compatible with Motorola SPI (CPOL=0, CPHA=0), and National Semiconductor Microwire specifications.

Functional waveforms are shown in and Figure 14. Detailed timing diagrams are shown in Figure 19 and Figure 20 in the electrical characteristics section. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK). Receive data bits are sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK.

The MT92303 supports Motorola half-duplex processor mode (CPOL=0 and CPHA=0). This means that during a write to the MT92303 by the Motorola-type processor, output data from the DATA1 pin must be ignored (by the processor). This also means that input data on the DATA2 pin is ignored by the MT92303 during a valid read by the Motorola processor. All data transfers through the microport are two bytes long. This requires the transmission of a Command/Address byte followed by the data byte to be written to or read from the addressed register. $\overline{CS}$ must remain low for the duration of this two-byte transfer.

As shown in and Figure 14 the falling edge of $\overline{CS}$ indicates to the MT92303 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation (read = 1, write = 0), and at what address.

The next 8 clock cycles are used to transfer the data byte between the MT92303 and the microcontroller. At the end of the two-byte transfer, $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as $\overline{CS}$ is high. Motorola/National processors use Most Significant Bit (MSB) first transmission.

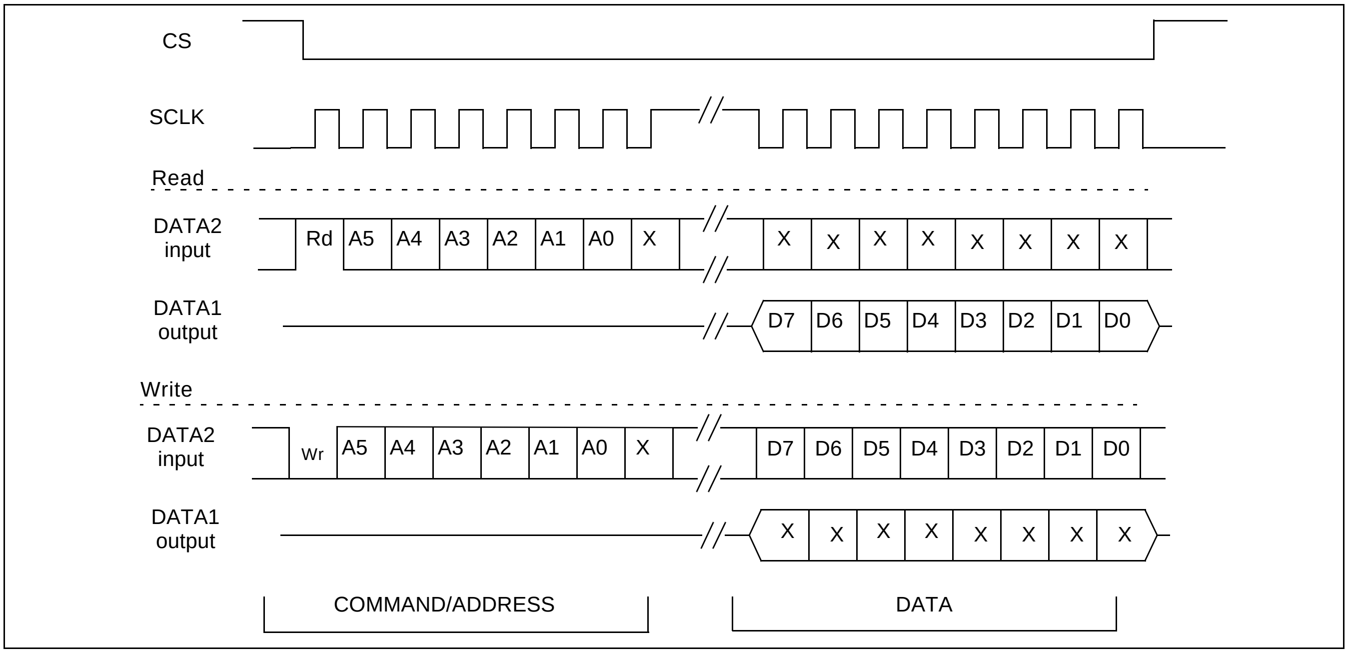


Figure 14 - Microport Waveform (Motorola/National mode)

Microport Timing Requirements

As shown in and Figure 20, there are several ‘sequencing’ requirements which must be met. The SCLK edges must not start until CS is active (low), and must complete before it is taken inactive (high). There are setup and hold time requirements between the DATA and SCLK signals.

Piping Into The DSP/Codec Registers

The MT92303 has a total of 25 internal registers which are written to via the serial microport. These are split into two groups which need to be accessed in different ways.

Most of the registers (0Ah to 19h) are directly accessed by the microport.

The other 10 (00h to09h), which are associated with the internal DSP/Codec engines, have their data temporarily ‘buffered’ by the microport, after which it needs to be piped into its final destination. This requires an extra 18 SCLK cycles which may be provided in several different ways as described in the following list and as shown in Figure 15.

A: This is the ‘normal’ microport operation for a ‘non-DSP’ register - 16 SCLK cycles are required.

B: This is the simplest way to write to a ‘DSP/Codec’ register - it requires 16+18 SCLK cycles per operation. Alternatively, SCLK may be allowed to run continuously rather than in bursts.

C: The extra SCLK cycles required for the ‘DSP/Codec’ write are provided by two further microport operations - notice that CS is **not** active for these. One method of achieving this is to arrange for the microport controller to write/read to another (non existent) peripheral i.e. not the MT92303. In this way, the SCLK cycles will be generated, but the MT92303 will not be ‘selected’.

D: The required SCLK cycles are provided by performing a ‘triple write’ to each ‘DSP/Codec’ register.

E: The required SCLK cycles are provided by performing a triple operation to each ‘DSP/Codec’ register. In this case, the two extra operations are ‘reads’ from the non existent register ‘3F’.

F: This method allows the programming to be carried out in fewer operations than the ‘triple operations’ described above. Each ‘DSP/Codec’ register is written-to twice, but it is important to notice that the sequence must end with a read/write operation to a ‘non-DSP’ register.

G: This method allows the programming to be carried out in the minimum number of operations, but is more complicated. Each ‘DSP/Codec’ register is written-to with a **single** operation, but notice that there is a sequencing requirement. The operations must alternate between the registers for DSP/Codec #0 and #1. In addition, the last ‘DSP/Codec’ operation must be followed by **two** read/write operations to a ‘non-DSP’ register.

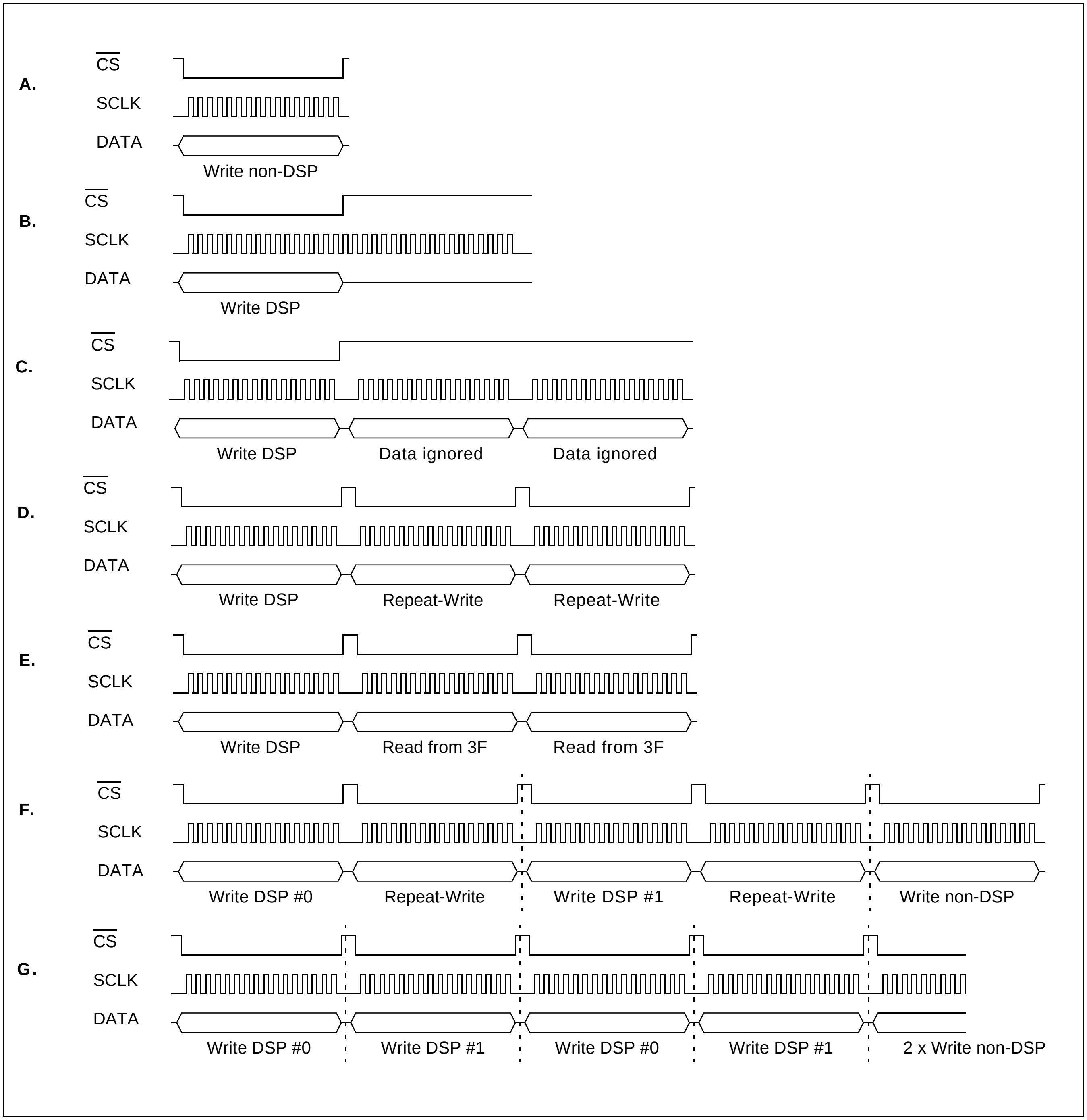


Figure 15 - Options For Writing To The DSP/Codec Register

System Clock

The MT92303 requires a ‘system’ clock signal which is used to run the internal DSP circuitry. The MT92303 is designed to work with several popular clock frequencies as shown in Table 7. The ‘system’ clock should be presented to the ‘SYSCLK’ input (standard digital input), and the appropriate on-chip register should be programmed with the chosen frequency.

System Clock MHz	Clocking Method	Required Frame Alignment Frequency
20.48	Direct	8kHz, synchronous
20.0	Direct	8kHz +/-400ppm
25.0	Direct	8kHz +/-320ppm
50.0	Direct	8kHz +/-320ppm
2.048	Internal PLL	8kHz, synchronous
4.096	Internal PLL	8kHz, synchronous
10.24	Internal PLL	8kHz, synchronous

Table 7 - SYSCLK Frequencies

Only the frequencies shown in Table 7 may be used - this is a requirement of the internal DAC’s and ADC’s which are of the ‘over-sampling’ type. The SYSCLK frequency needs to be a multiple of the 8kHz frame rate, and also the internal sampling clocks of the DAC’s and the ADC’s.

Some of the SYSCLK frequency options use an internal PLL to multiply the clock up to 20.48MHz, but the faster SYSCLK frequencies are used directly by the DSP circuitry. When ‘Direct’ SYSCLK frequencies are used, the clock signal must have a mark-to-space ratio between 40:60 and 60:40.

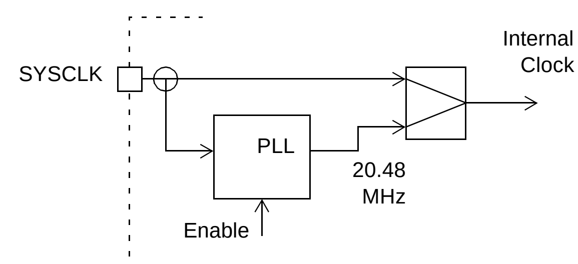


Figure 16 - SYSCLK Input and PLL

Those SYSCLK frequencies which are multiples of 2.048MHz are expected to be derived from the same source as that which provides the PCM Interface’s ‘Frame Alignment’ signal (F0i/FSC/SC2). The two signals must be synchronous - one of the ways that this can be achieved is by using the *same* clock signal for both SYSCLK and C4i/DCL/SCK.

The other SYSCLK frequencies are intended for use in VoIP applications where Ethernet clocks may already be available. The MT92303 contains a digital re-synchronization circuit which means that the 20.0, 25.0 or 50.0MHz SYSCLK does not need to be synchronous with the ‘Frame Alignment’ signal. However, in these cases, there are minimum requirements for the accuracy of the 8kHz ‘Frame Alignment’ frequency, as shown in Table 7.

It is important to note that the accuracy figures in Table 7 (e.g. 8kHz +/-320ppm for 25MHz System Clock) are defining the *relative* inaccuracy of the two clocks (8kHz and 25MHz in this example). The two clock frequencies must share the 320ppm of allowable inaccuracy (e.g. 8kHz +/-160ppm and 25MHz +/-160ppm).

The internal PLL must be enabled whenever it is required. This is controlled by the same register as is used to select the SYSCLK frequency. The PLL will take <1ms to lock onto the SYSCLK signal - during this time the ‘DSP’ circuitry will be clocked at the wrong frequency (slower, or faster), and consequently the PCM data should not be relied upon until the PLL has settled. When the PLL is not needed, or when a ‘low power’ mode is required, then the PLL should be disabled.

The PLL should not be enabled until the SYSCLK clock signal has been applied. It is acceptable to simultaneously select the SYSCLK frequency and enable the PLL. After a System Reset, the MT92303 will be in a ‘Direct’ clocking mode (20.48MHz Direct as shown in Table 7), and consequently must be put into a mode where the PLL is programmed to multiply the SYSCLK frequency by the correct amount, and where the PLL is ‘enabled’ (if the PLL is required).

System Reset Options

The MT92303 has a ‘RESET’ mode in which all the Control Registers, the DSP, and all other latched functions are ‘reset’. This ‘RESET’ mode may be initiated in three different ways:

- Powering-up the device
- Using the active-low ‘RESETB’ pin
- Setting the ‘SW_RESET’ bit in the appropriate register

The ‘software’ reset is programmed via the Microport Interface, and is cleared by another *dummy* Microport operation. This must be a ‘read’ operation from register address 3F (a non-existent register).

Power-Down Mode

The individual circuits of the MT92303 are capable of being powered-down when not needed. This allows the operating current to be minimized, and it also allows the whole chip to be powered-down into a micro-power state if required.

The circuits are powered-down under the control of the relevant register bits. In general, the circuitry is powered-down after a power-on-reset or hardware or software reset, and is usually ‘enabled’ when required. To put the MT92303 into micro-power mode, all of the circuits listed below need to be ‘disabled’ by setting the register bits low. For absolute minimum power consumption, the System Clock must also be stopped.

- Audio Interfaces #0 to #3 (‘EN_AUDIO’ x4)
- TX analog #0 and #1 (‘EN_TX’ x2)
- Voltage reference (‘EN_VREF’ x1)
- PLL (‘EN_PLL’ x1)
- Codecs #0 and #1 (‘EN_CODEC’ x2)

MT92303 Programming & Registers

All operating modes, power up/down, gain levels and muting, electret biasing, filter cut-off's etc. are set by the contents of the registers shown below. These are all accessed via the microport. Some of the registers are write-only, some are read-write, and the 'Status' register is read-only. The 'hex' addresses and read/write access are shown at the top of each table. Note that most of the registers are duplicated - there are generally 2 addresses for registers which control the Codecs and 4 addresses for those which control the Audio Interfaces.

Register Defaults

The MT92303 has an on-chip 'Power On Reset' circuit which is used to clear and initialize the circuitry whenever power is applied to the device. The RESETB pin may also be used to provide a 'hardware' reset which produces the same effect. In this state, all the register bits are reset to '0'

Figure 21 shows a flow diagram with a suggested register programming sequence. There are several 'sequencing' requirements shown in the flow diagram - it is important that these are followed.

Address 00h/01h Write only		**DSP/Codec: Control (Registers x2)**
0	MUTE_V	'DSP' RX Mute
1	MUTE_S	'DSP' Sidetone Mute
2	PCM	0=Linear 1=Companded
3	u/A Law	0=A Law 1=u Law
4-7	-	UNUSED (Don't care)

Address 02h/03h Write only		**DSP/Codec: Enable and RX DSP Gain (Registers x2)**
0	EN_CODEC	Enable Codec
1	VOL[0]	'DSP' RX Volume Control from -21dB to 0dB in 3dB steps. See table below
2	VOL[1]	
3	VOL[2]	
4-7	-	UNUSED (Don't care)

VOL[2:0]	**GAIN dB**
000	0
001	-3
010	-6
011	-9
100	-12
101	-15
110	-18
111	-21

Table 8 - DSP RX Volume Control

Address 04h/05h Write only		DSP/Codec: RX Hi-Pass-Filter (Registers x2)
0	RXHPF[0]	Cut Off Frequency of RX Path ‘DSP’ Hi Pass Filter (1st order filter). See table below
1	RXHPF[1]	
2	RXHPF[2]	
3	SCAN[0]	Scan-path test modes. (Defaults to ‘00’. Do not over-write with different value)
4	SCAN[1]	
5-7	-	UNUSED (Don’t care)

RXHFP[2:0]	-3dB Frequency (Hz)
000	0
001	40
010	100
011	150
100	200
101	300
110	400
111	Invalid

Table 9 - RX path DSP Hi Pass Filter

Address 06h/07h Write only		DSP/Codec: Sidetone Gain (Registers x2)
0	DSP TEST	DSP bus access test mode. (Defaults to ‘0’. Do not over-write with different value)
1	STG[0]	Sidetone gain. See table below
2	STG[1]	
3	STG[2]	
4	STG[3]	
5-7	-	UNUSED (Don’t care)

STG[3:0]	GAIN (dB)	STG[3:0]	GAIN (dB)
0000	-39	1000	-15
0001	-36	1001	-12
0010	-33	1010	-9
0011	-30	1011	-6
0100	-27	1100	-3
0101	-24	1101	0
0110	-21	1110	+3
0111	-18	1111	+6

Table 10 - Sidetone Gain

Address 08h/09h Write only		DSP/Codec: DSP Test (Registers x2)
0	DSPTEST[0]	RESERVED (Defaults to ‘0’. Do not over-write with different value)
1	DSPTEST[1]	RESERVED (Defaults to ‘0’. Do not over-write with different value)
2	DSPTEST[2]	RESERVED (Defaults to ‘0’. Do not over-write with different value)
3-7	-	UNUSED (Don’t care)

Address 0Ah - 0Bh Read/Write		Audio Interface: TX Gain (Registers x2)
0	TXG[0]	Programmable TX gain 0 to +46.5dB in 1.5dB steps. See table below TXG[4] controls whether or not the ‘pre-amp’ is used
1	TXG[1]	
2	TXG[2]	
3	TXG[3]	
4	TXG[4]	
5-7	-	UNUSED (Don’t care)

TXG[4:0]	GAIN dB	TXG[4:0]	GAIN dB	TXG[4:0]	GAIN dB	TXG[4:0]	GAIN dB
00000	0	01000	12	10000	24	11000	36
00001	1.5	01001	13.5	10001	25.5	11001	37.5
00010	3	01010	15	10010	27	11010	39
00011	4.5	01011	16.5	10011	28.5	11011	40.5
00100	6	01100	18	10100	30	11100	42
00101	7.5	01101	19.5	10101	31.5	11101	43.5
00110	9	01110	21	10110	33	11110	45
00111	10.5	01111	22.5	10111	34.5	11111	46.5

Table 11 - TX Path Analog Gain

Address 0Ch - 0Fh Read/Write		Audio Interface: RX Analog Gain and Electret Bias (Registers x4)
0	RXG[0]	Programmable RX ‘analog’ gain -28dB to +2.0dB in 2dB steps (available for all four Audio Interfaces). See table below Register for Audio Interface #0 also defines ‘AUXTONE’ gain between -26.5dB and +5.9dB in approximate 2dB steps. See table below
1	RXG[1]	
2	RXG[2]	
3	RXG[3]	
4	EB[0]	Programmable Electret Microphone Bias 0V to 2.5V in 163mV steps. See table below Available for Audio Interfaces #3, #2 and #0
5	EB[1]	
6	EB[2]	
7	EB[3]	

RXG [3:0]	GAIN (dB)	RXG [3:0]	GAIN (dB)
0000	-28	1000	-12
0001	-26	1001	-10
0010	-24	1010	-8
0011	-22	1011	-6
0100	-20	1100	-4
0101	-18	1101	-2
0110	-16	1110	0
0111	-14	1111	+2

Table 12 - RX ‘Analog’ Gain

RXG0 [3:0]	AUX GAIN (dB)	RXG0 [3:0]	AUXGAIN (dB)
0000	-26.5	1000	-10.1
0001	-24.5	1001	-7.9
0010	-22.5	1010	-5.8
0011	-20.4	1011	-3.6
0100	-18.4	1100	-1.4
0101	-16.3	1101	+1.0
0110	-14.2	1110	+3.4
0111	-12.2	1111	+5.9

Table 13 - #0 AUXTONE Gain

EB [3:0]	Bias V	EB [3:0]	Bias V
0000	0.04	1000	1.34
0001	0.21	1001	1.51
0010	0.37	1010	1.67
0011	0.53	1011	1.84
0100	0.69	1100	2.00
0101	0.85	1101	2.16
0110	1.02	1110	2.32
0111	1.18	1111	2.49

Table 14 - Electret Bias

Address 10h Read/Write		Audio Interface: Enable (Register x1)
0	EN_AUDIO_0	Enable Audio Interfaces (RX 'analog' circuitry, Electret bias, Microphone detect, Auxtone)
1	EN_AUDIO_1	
2	EN_AUDIO_2	
3	EN_AUDIO_3	
4	EN_VREF	Enable Voltage Reference (needed for all analog functions)
5	EN_TX0	Enable TX 'analog' circuitry. Also initiates the 'TX offset correction' routine. **Important Note**: There are several requirements which must be met before this routine can operate correctly. See explanation in section 'Automatic DC Offset Cancellation (TX)'
6	EN_TX1	
7	-	UNUSED (Don't care)

Address 12h/13h Read/Write		PCM Interface: Codec Channel Allocation (Register x2)
0	CHAN[0]	Codec-Channel Allocation ST-Bus mode: (0 to 31) e.g. CHAN[4:0] = 01110 = Channel 14 GCI mode: (0 to 7) e.g. CHAN[4:0] = XX110 = Channel 6 SSI mode: ignored
1	CHAN[1]	
2	CHAN[2]	
3	CHAN[3]	
4	CHAN[4]	
5-7	-	UNUSED (Don't care)

Address 14h Read/Write		PCM Interface: Status Channel Allocation (Register x1)
0	CHAN[0]	Status-Channel Allocation ST-Bus mode: (0 to 31) e.g. CHAN[4:0] = 01110 = Channel 14 GCI mode: (0 to 7) e.g. CHAN[4:0] = XX110 = Channel 6 SSI mode: ignored
1	CHAN[1]	
2	CHAN[2]	
3	CHAN[3]	
4	CHAN[4]	
5-7	-	UNUSED (Don't care)

Address 15h Read/Write		General: Mode Control (Register x1)
0	PCM_BUS[0]	Selects PCM Data Interface 00 = ST-Bus, 01 = GCI, 10 = SSI
1	PCM_BUS[1]	
2	MUTEMODE3[0]	Audio Interface #3: Mic Mute mode control (see section 'Microphone Mute Detect' and table below)
3	MUTEMODE3[1]	
4	MUTEMODE2[0]	Audio Interface #2: Mic Mute mode control (see section 'Microphone Mute Detect' and table below)
5	MUTEMODE2[1]	
6	MUTE[0]	Software mute for Audio Interface #0
7	MUTE[1]	Software mute for Audio Interface #1

MUTEMODE[1:0]	Mute Operation (see Figure 9)
00	Microphone path enabled (normal operation). ‘Mic Mute Detect’ signal ignored
01	Microphone path disabled (muted) while ‘Mic Mute Detect’ signal is high, and enabled while low
10	Microphone path disabled (muted) while ‘Mic Mute Detect’ signal is high, **but must be re-enabled by the external controller**
11	Microphone path disabled (muted). ‘Mic Mute Detect’ signal ignored

Table 15 - Mute Modes

Address 16h Read/Write		General: System Clock Frequency, PLL and Software Reset (Register x1)
0	FREQ[0]	System Clock frequency, ‘SYSCLK’. See table below **Note**: Some frequencies need the internal PLL to be enabled
1	FREQ[1]	
2	FREQ[2]	
3	EN_PLL	Enable PLL (only required for some SYSCLK frequencies). Allow 1ms to settle
4	SW_RESET	‘Software Reset’ - see explanation in section ‘System Reset Options’
5-7	-	UNUSED (Don’t care)

FREQ [2:0]	System Clock (MHz)	Clocking Method	PLL Multiplier
000	20.48	Direct (PLL output not used)	x10
001	20.0	Direct (PLL output not used)	x5
010	25.0	Direct (PLL output not used)	x2
011	50.0	Direct (PLL output not used)	x2
100	2.048	Internal PLL	x10
101	4.096	Internal PLL	x5
110	10.24	Internal PLL	x2
111	10.24 (spare)	Internal PLL	x2

Table 16 - System Clock Frequencies

Address 17h Read/Write		General: Test (Register x1)‡
0	TEST[1:0]	RESERVED‡ for ‘gemulation mode’ testing
1		
2	TEST[3:2]	RESERVED‡ for internal signal testing via DTSO pin. 01 = Internal SYSCLK (PLL output in some modes)
3		
4	0	RESERVED‡
5	0	
6	0	
7	0	

‡Defaults to all-zero’s. Do not over-write with different values

Address 18h Read/Write		General: Test TX Analog (Register x1)‡
0	PDVC	RESERVED‡ for production testing
1	PDSD	
2	PDDAC	
3	TCALVG	
4	TCALMA	
5	TSTVG	
6	TSTAA	
7	-	

Address 19h Read only		Audio Interface: Status (Register x1)
0	MUTEDET3	Audio Interface #3: ‘Mic Mute Detect’ signal
1	MUTE3	Audio Interface #3: Microphone Channel is Muted (may need to be actively un-muted)
2	MUTEDET2	Audio Interface #2: ‘Mic Mute Detect’ signal
3	MUTE2	Audio Interface #2: Microphone Channel is Muted (may need to be actively un-muted)
4	MIC3	Audio Interface #3: ‘Mic Presence Detect’ signal
5	MIC2	Audio Interface #2: ‘Mic Presence Detect’ signal
6-7	-	UNUSED (Don’t care)

AC/DC Electrical Characteristics

‡ Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Absolute Maximum Ratings‡

Characteristics	Min	Max	Units	Comments
Storage Temperature	-55	+150	degC	
Supply Voltage	-0.3	5.0	V	< 2 minutes
	-0.3	3.6	V	Continuous
Pin voltage relative to VDD		+0.3	V	
Pin voltage relative to GND or SUB	-0.3		V	

Recommended Operating Conditions

Characteristics	Min	Max	Units	Comments
Ambient Temperature	-40	+85	°C	
Supply Voltage Vdd	3.0	3.6	V	

General Characteristics

Characteristics	Min	Typ‡	Max	Units	Comments
Supply Current		13	23	mA	Operating. No output loads
			10	uA	Powered down
Digital Inputs: lower threshold			0.8	V	
Digital Inputs: upper threshold	2.0			V	
Digital Outputs: lower level			0.4	V	Sinking 6mA
Digital Outputs: upper level	0.8*VDD				Sourcing 6mA

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

RX Path Characteristics

All parameters are measured differentially between the ‘EARP’ and ‘EARN’ pins. DSP gain is set to 0dB unless otherwise stated.

Characteristics	Min	Typ‡	Max	Units	Comments
Output level for 0dBm0	0.83	0.90	0.97	V rms	Analog gain set to 0dB
		35.8		mV rms	Analog gain set to -28dB
Driver output power	66			mW rms	1kHz sinewave, <1% THD, 32 Ohm load
Speaker output power (Audio Interface #0 only)	150			mW rms	1kHz sinewave, <1% THD, 16 Ohm load
Output resistance		1		Ohms	1kHz sinewave
Analog gains		-28 to +2		dB	16 gain values available
Analog gain error	-1.0	0	+1.0	dB	Analog gain -28dB to +2dB, 1kHz, 0dBm0
Analog gain step size		2		dB	
Idle channel noise		-68		dBm0p	u/A law mode. Analog gain set to 0dB
		-68			Linear mode. Analog gain set to 0dB
DC offset voltage	-50		+50	mV	Analog gain 0dB

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AUXTONE Path Characteristics

All parameters are measured differentially between the 'EAR0P/SPEAKERP' and 'EAR0N/SPEAKERN' pins unless otherwise stated.

Characteristics	Min	Typ‡	Max	Units	Comments
Gain		-26.5 to +5.9		dB	16 gain values available
Gain step size		2		dB	Step sizes not all equal
Maximum gain setting	-0.5	5.9	+0.5	dB	1kHz, 1V rms sinewave
Input DC bias		VDD/2		V	AUXTONE input
AUXTONE input resistance (AC)		83		kOhms	Minimum gain setting
		29		kOhms	Maximum gain setting

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

TX Path Characteristics

All parameters are referred to the differential signal between the 'MICP' and 'MICN' pins unless otherwise stated.

Characteristics	Min	Typ‡	Max	Units	Comments
Input level for 0dBm0	0.56	0.611	0.67	V rms	Gain set to 0dB
		2.89		mV rms	Gain set to 46.5dB
Input common-mode bias		VDD/2		V	DC bias on each input, relative to GND
Input resistance (AC)		107		kOhms	Gain 0dB to 10.5dB
		54		kOhms	Gain 12dB to 22.5dB
		80		kOhms	Gain 24dB to 46.5dB
Gains		0 to +46.5		dB	32 gain values available
Gain error	-0.75	0	+0.75	dB	Gain 0dB to 46.5dB, 1kHz, 0dBm0
Gain step size		1.5		dB	
Idle channel, output noise		-77		dBm0	Output noise. Gain set to 0dB
		-53		dBm0	Output noise. Gain set to 46.5dB

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Electret Bias, Mic Presence and Mic Mute Detect Characteristics

All parameters measured at the ‘MICBIAS’ pin relative to GND.

Characteristics	Min	Typ‡	Max	Units	Comments
Electret bias voltage ‘EBV’	0.9 * Typ - 50mV	0.04 to 2.49	1.1 * Typ + 50mV	V	16 levels available. See Registers 0C-0F
Output noise		25		uV rms	300-3400Hz
Drive current capability	1			mA	Source current
Output resistance		2		Ohms	At 1kHz
Supply rejection		60		dB	At 1kHz
‘Presence’ detect threshold (rising)	Typ - 20mV	0.04 * EBV	Typ + 20mV	V	Derived from electret bias voltage
‘Presence’ detect threshold (falling)		0.03 * EBV			
‘Mute’ detect threshold (rising)	0.97 * Typ - 10mV	0.40 * EBV	1.03* Typ + 10mV	V	Derived from electret bias voltage
‘Mute’ detect threshold (falling)		0.35 * EBV			

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

PCM Serial Data Interface Timings (ST-Bus)

Characteristics	Sym	Min	Typ	Max	Units	Test Notes
$\overline{\text{C4i}}$ Period	t_{C4P}	243.9	244.1	244.4	ns	
$\overline{\text{C4i}}$/DCL/SCK Clock High	t_{SCH}, t_{C4H}	90			ns	
$\overline{\text{C4i}}$/DCL/SCK Clock Low	t_{SCL}, t_{C4L}	90			ns	
$\overline{\text{F0i}}$ / FSC Setup	t_{F0iS}	20		150	ns	
$\overline{\text{F0i}}$ / FSC Hold	t_{F0iH}	20		150	ns	
ST-BUS/GCI Data Input Hold time	t_{DSH}	20			ns	
ST-BUS/GCI Data Input Setup time	t_{DSS}	20			ns	
ST-BUS/GCI Data Output delay	t_{DSD}			80	ns	C_L=150pF
ST-BUS/GCI Output Active to High Impedance	t_{ASHZ}			80	ns	C_L=150pF

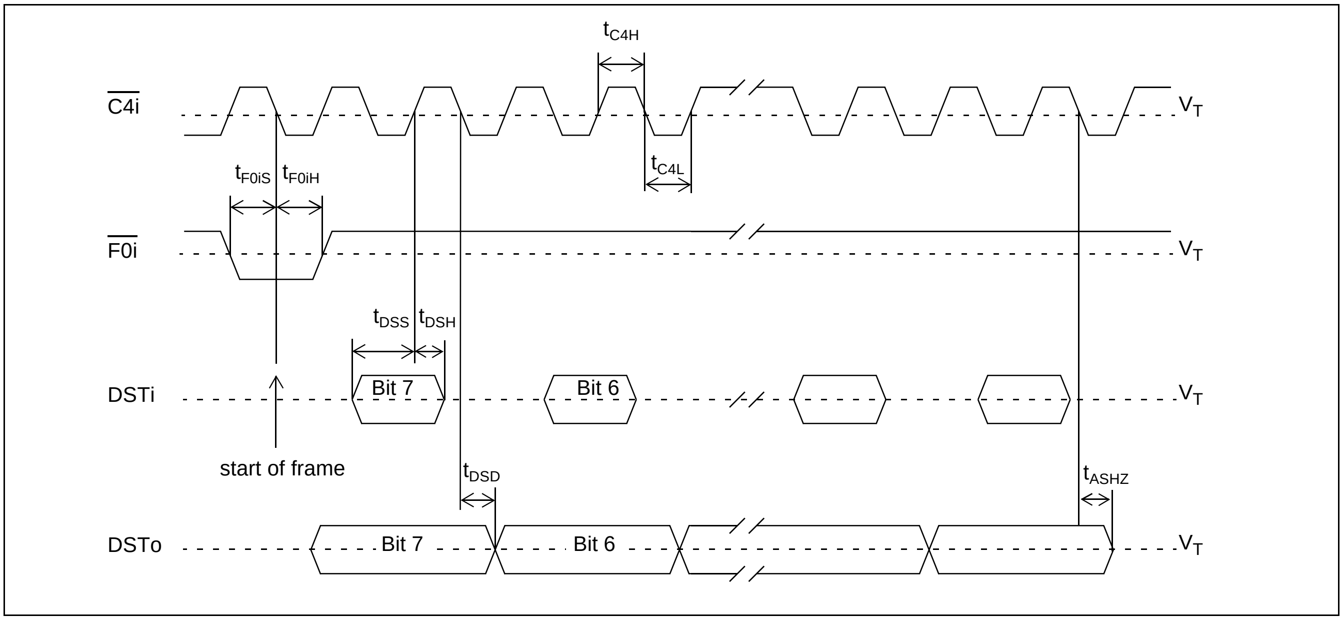


Figure 17 - PCM ST-Bus Data Port Timing

PCM Serial Data Interface Timings (GCI)

Characteristics	Sym	Min	Typ	Max	Units	Test Notes
DCL Period	t_{CKP}	244		651	ns	
$\overline{\text{C4i}}$/DCL/SCK Clock High	t_{SCH}, t_{C4H}	90			ns	
$\overline{\text{C4i}}$/DCL/SCK Clock Low	t_{SCL}, t_{C4L}	90			ns	
$\overline{\text{F0i}}$ / FSC Setup	t_{F0iS}	20		150	ns	
$\overline{\text{F0i}}$ / FSC Hold	t_{F0iH}	20		150	ns	
ST-BUS/GCI Data Input Hold time	t_{DSH}	20			ns	
ST-BUS/GCI Data Input Setup time	t_{DSS}	20			ns	
GCI FSC to Data Delay (first bit)	t_{SD}			80	ns	C_L=150pF
ST-BUS/GCI Data Output delay	t_{DSD}			80	ns	C_L=150pF
ST-BUS/GCI Output Active to High Impedance	t_{ASHZ}			80	ns	C_L=150pF

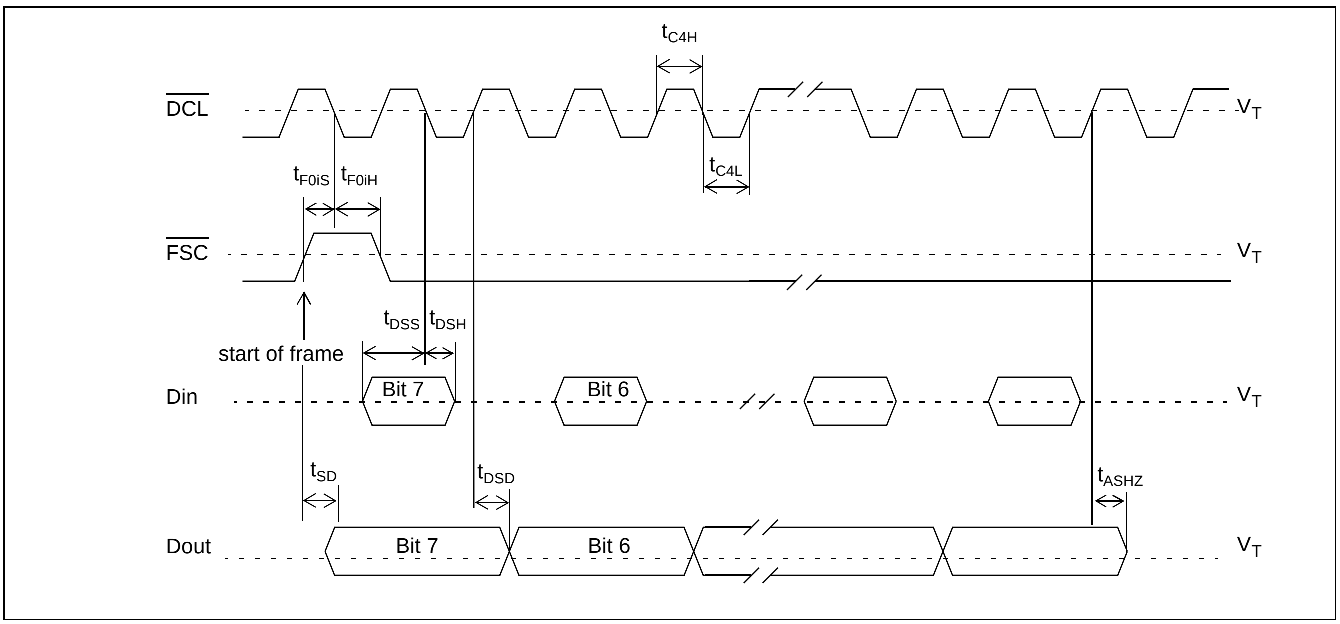


Figure 18 - PCM GCI Data Port Timing

PCM Serial Data Interface Timings (SSI)

Characteristics	Sym	Min	Typ	Max	Units	Test Notes
SCK Period	t_{SCP}	244		1953	ns	
$\overline{C4i}$/DCL/SCK Clock High	t_{SCH}, t_{C4H}	90			ns	
$\overline{C4i}$/DCL/SCK Clock Low	t_{SCL}, t_{C4L}	90			ns	
SSI Enable Strobe to Data Delay (first bit)	t_{SD}			80	ns	C_L=150pF
SSI Data Output Delay (excluding first bit)	t_{DD}			80	ns	C_L=150pF
SSI Output Active to High Impedance	t_{AHZ}			80	ns	C_L=150pF
SSI Enable Strobe Signal Setup	t_{SS}	70		t_{SCP}	ns	
SSI Enable Strobe Signal Hold	t_{SH}	15		t_{SCP}-10	ns	
SSI Data Input Setup	t_{SDS}	10			ns	
SSI Data Input Hold	t_{SDH}	15			ns	

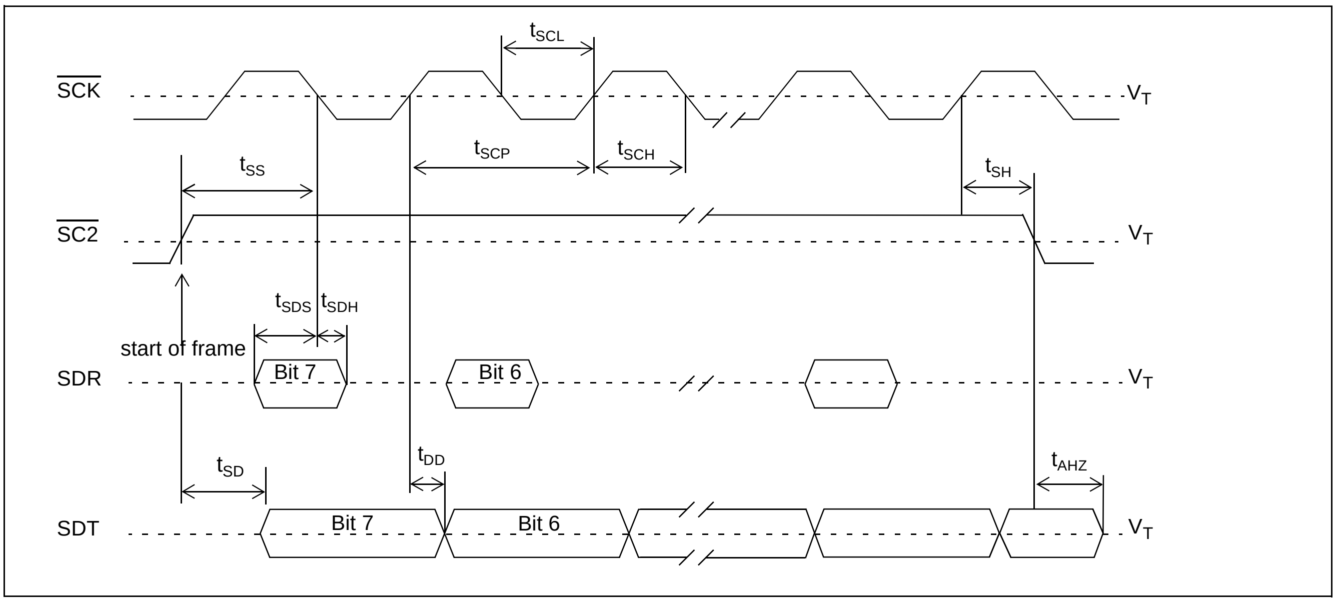


Figure 19 - PCM SSI Data Port Timing

Microport Timings

Characteristics	Sym	Min	Typ	Max	Units	Test Notes
Input Data Setup	t_{IDS}	100			ns	
Input Data Hold	t_{IDH}	30			ns	
Output Data Delay	t_{ODD}			100	ns	C_L=150pF
Serial Clock Period	t_{SCP}	500			ns	
SCLK Pulse Width High	t_{SCH}	250			ns	
SCLK Pulse Width Low	t_{SCL}	250			ns	
$\overline{CS}$ Setup-Motorola	t_{CSSM}	100			ns	
$\overline{CS}$ Hold	t_{CSH}	100			ns	
$\overline{CS}$ to Output High Impedance	t_{OHZ}			100	ns	C_L=150pF

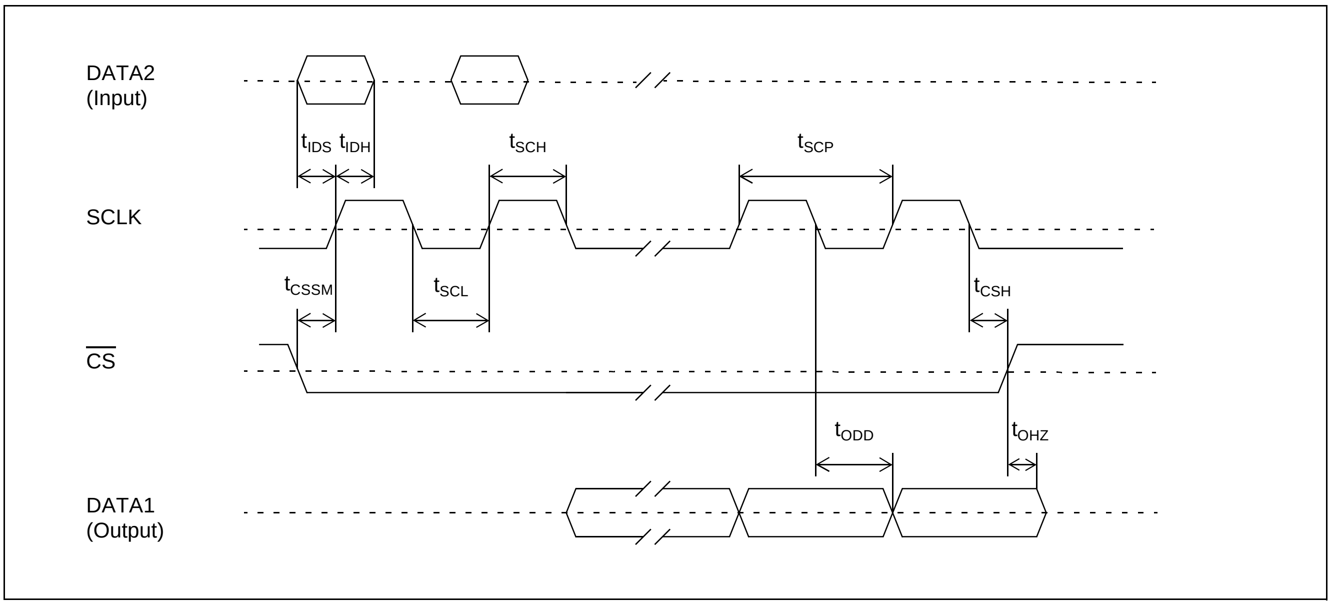
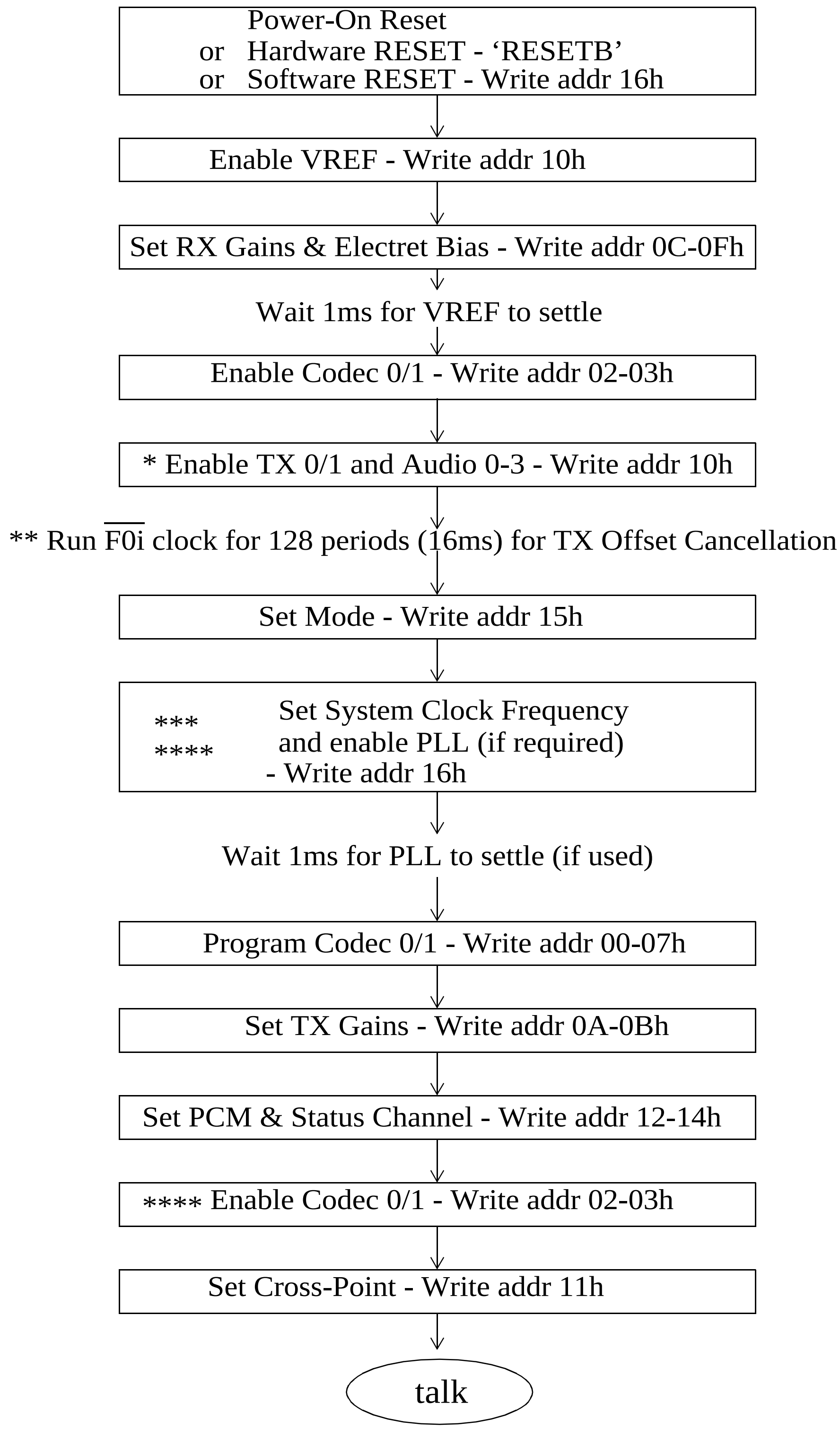


Figure 20 - Motorola/National Serial Microport Timing



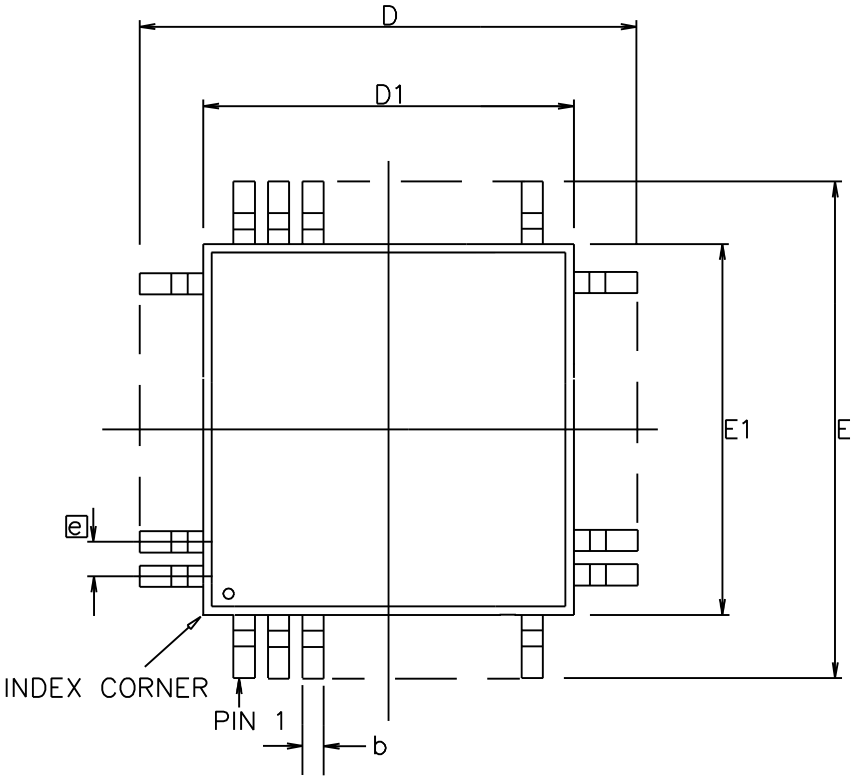
* TX 0/1 must be enabled after VREF has settled.

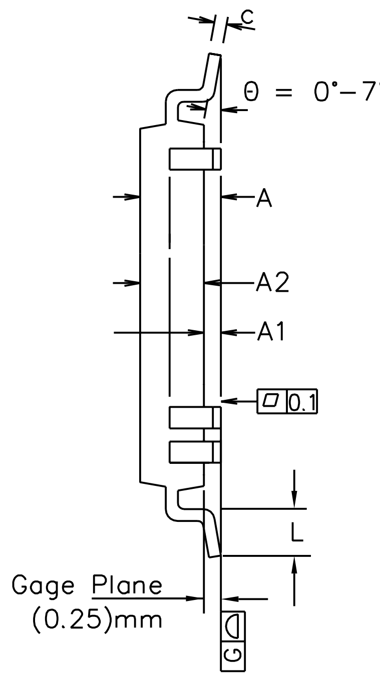
** C4I_ must be running during TX Offset Cancellation.

*** SYSCLK must be present before PLL is enabled.

**** After a Frequency register write, each Codec must be enabled or re-enabled.

Figure 21 - Suggested Microport Programming Sequence





Symbol	Control Dimensions in millimetres MIN	Control Dimensions in millimetres MAX		Altern. Dimensions in inches MIN	Altern. Dimensions in inches MAX
A	–	2.45		–	0.096
A1	0.00	0.25		0.000	0.010
A2	1.80	2.20		0.071	0.087
D	13.20 BSC			0.520 BSC	
D1	10.00 BSC			0.394 BSC	
E	13.20 BSC			0.520 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.73	1.03		0.029	0.041
e	0.80 BSC.			0.031 BSC.	
b	0.29	0.45		0.011	0.018
c	0.11	0.23		0.004	0.009
	Pin features				
N	44				
ND	11				
NE	11				
NOTE	SQUARE				

Conforms to JEDEC MS-022 AB-1 Iss. B

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.010 mm max.

ISSUE	1	2	3	4
ACN	201346	205424	207059	212437
DATE	25Oct96	22Oct98	29Jun99	25Mar02
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP

Package Code QB

Package Outline for 44 lead MQFP (10 x 10 x 2.0mm) 3.2mm Footprint

GPD00231

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com